

PG132-A02

370W, FH Std PCB, 384b, GDDR6x 2CH X16
DP + DP + DP + HDMI/DP

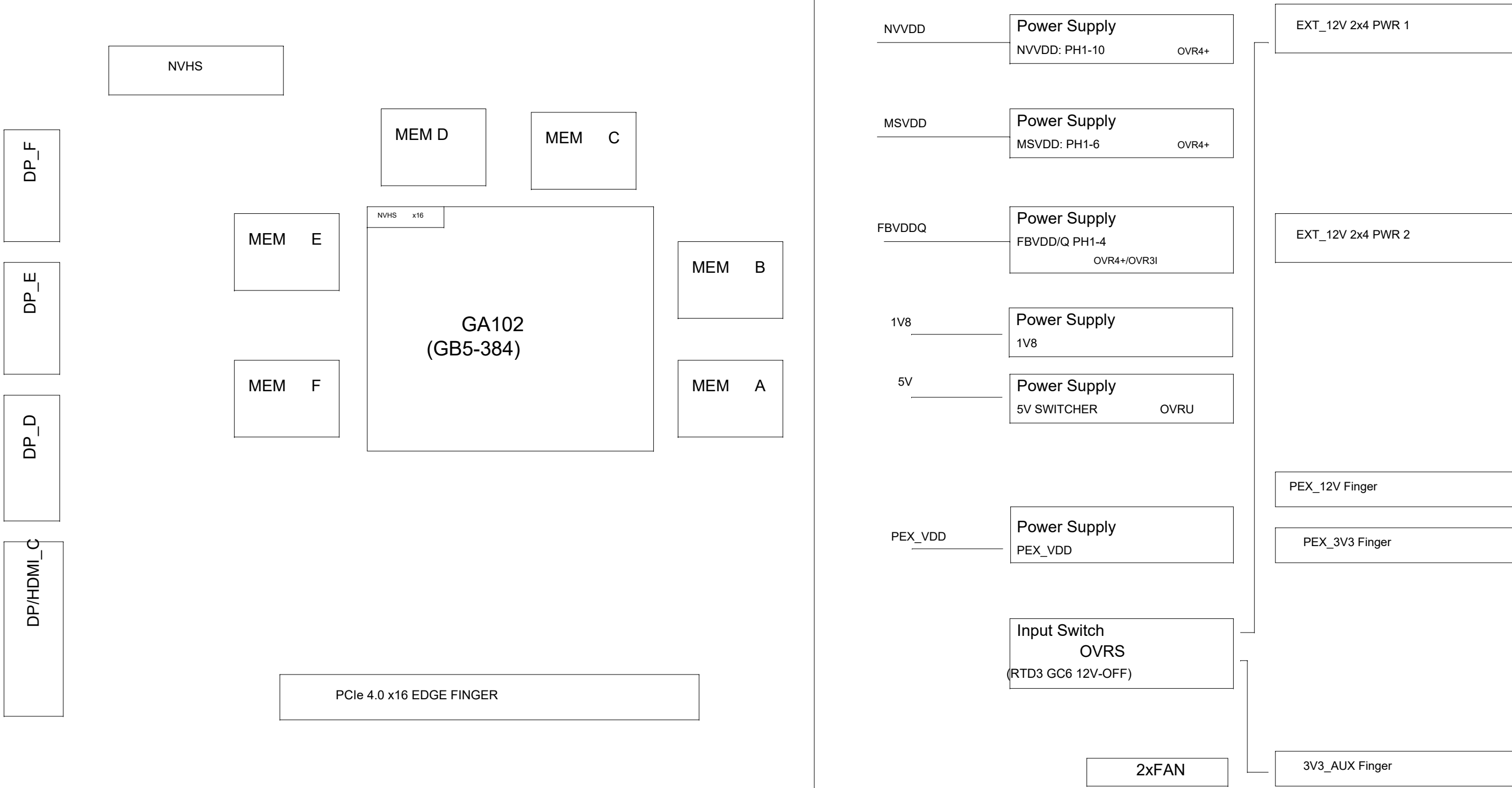
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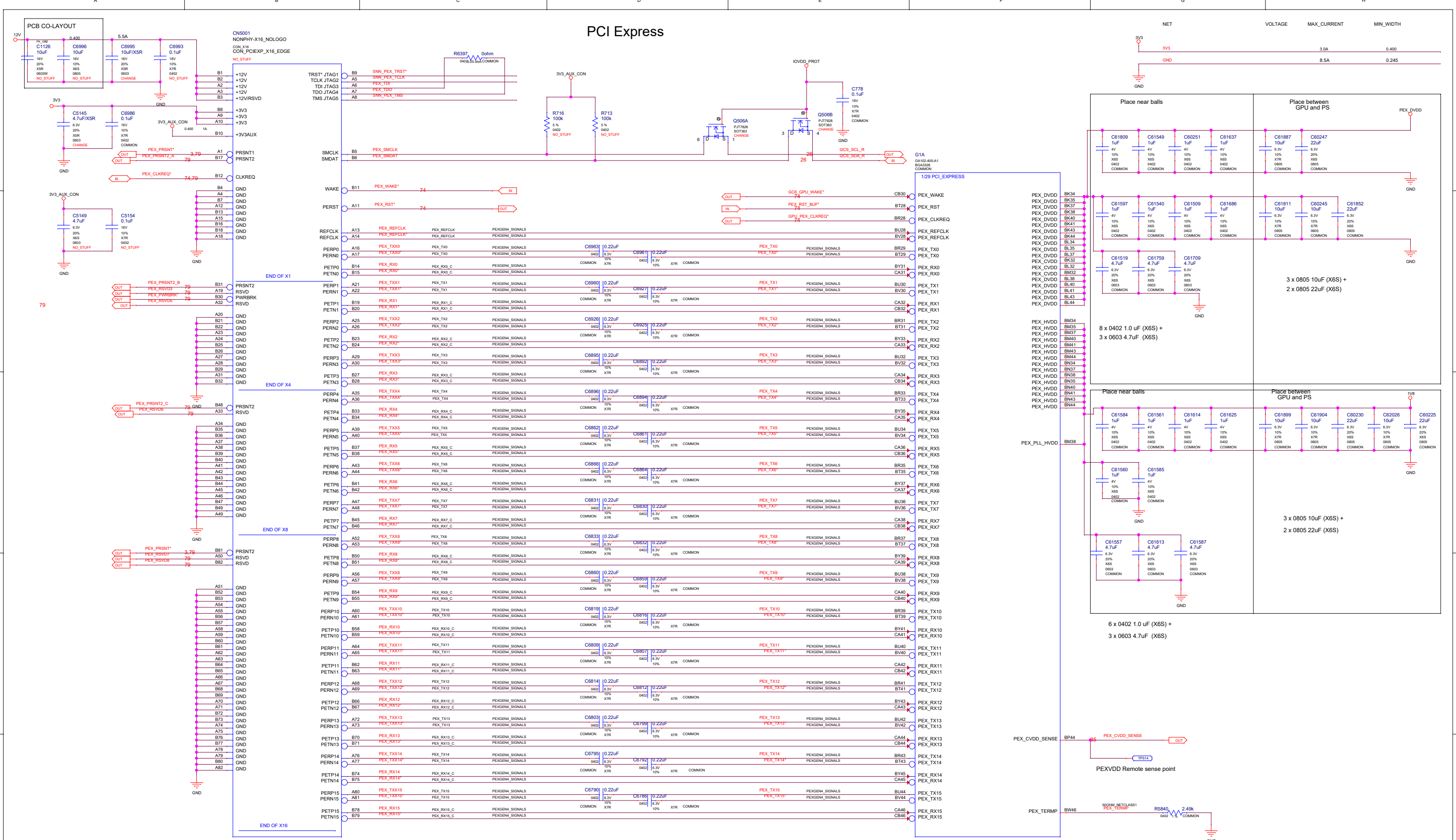
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Block Diagram






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ASSEMBLY
PAGE DETAIL

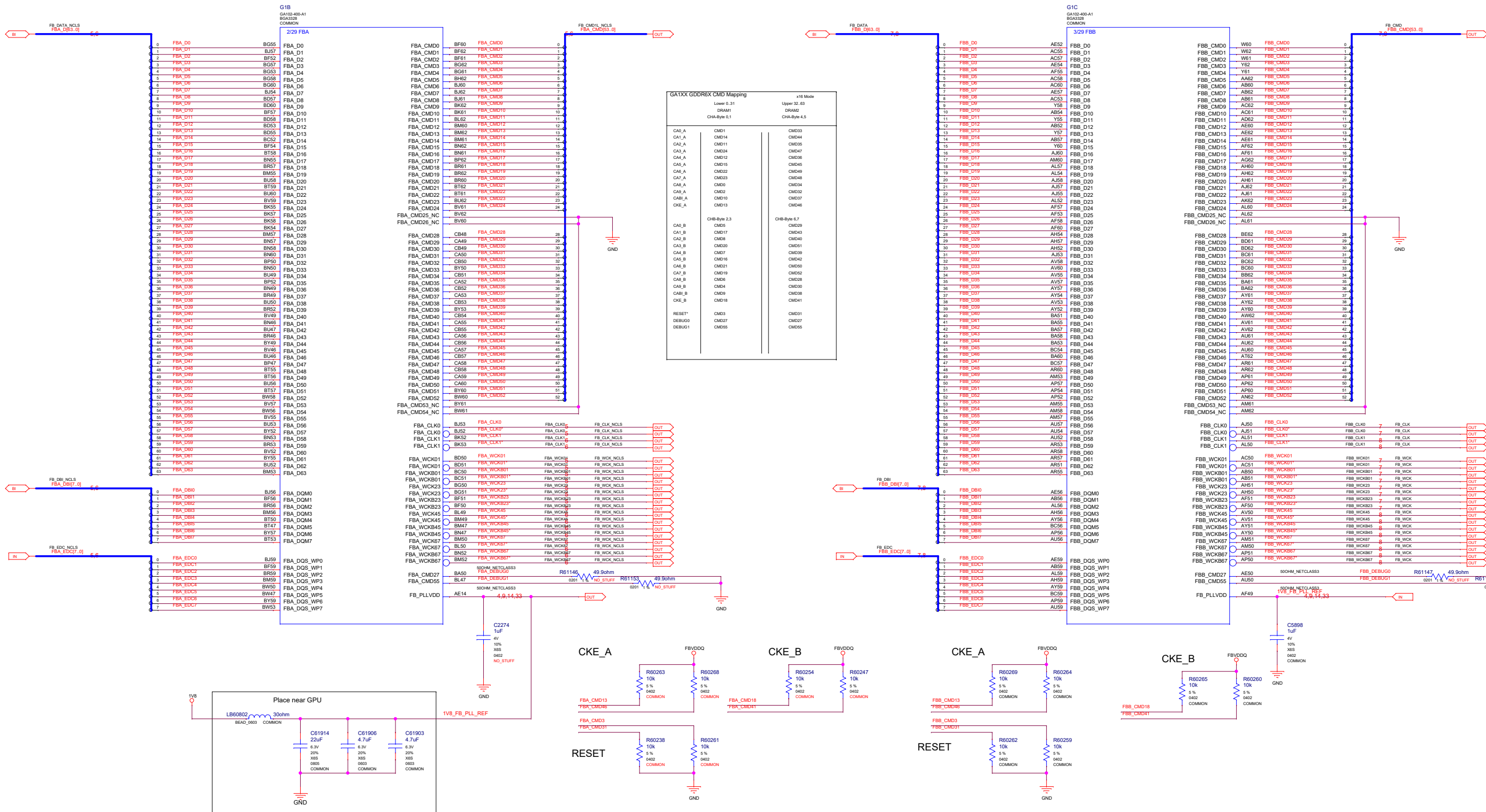
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PCI EXPRESS



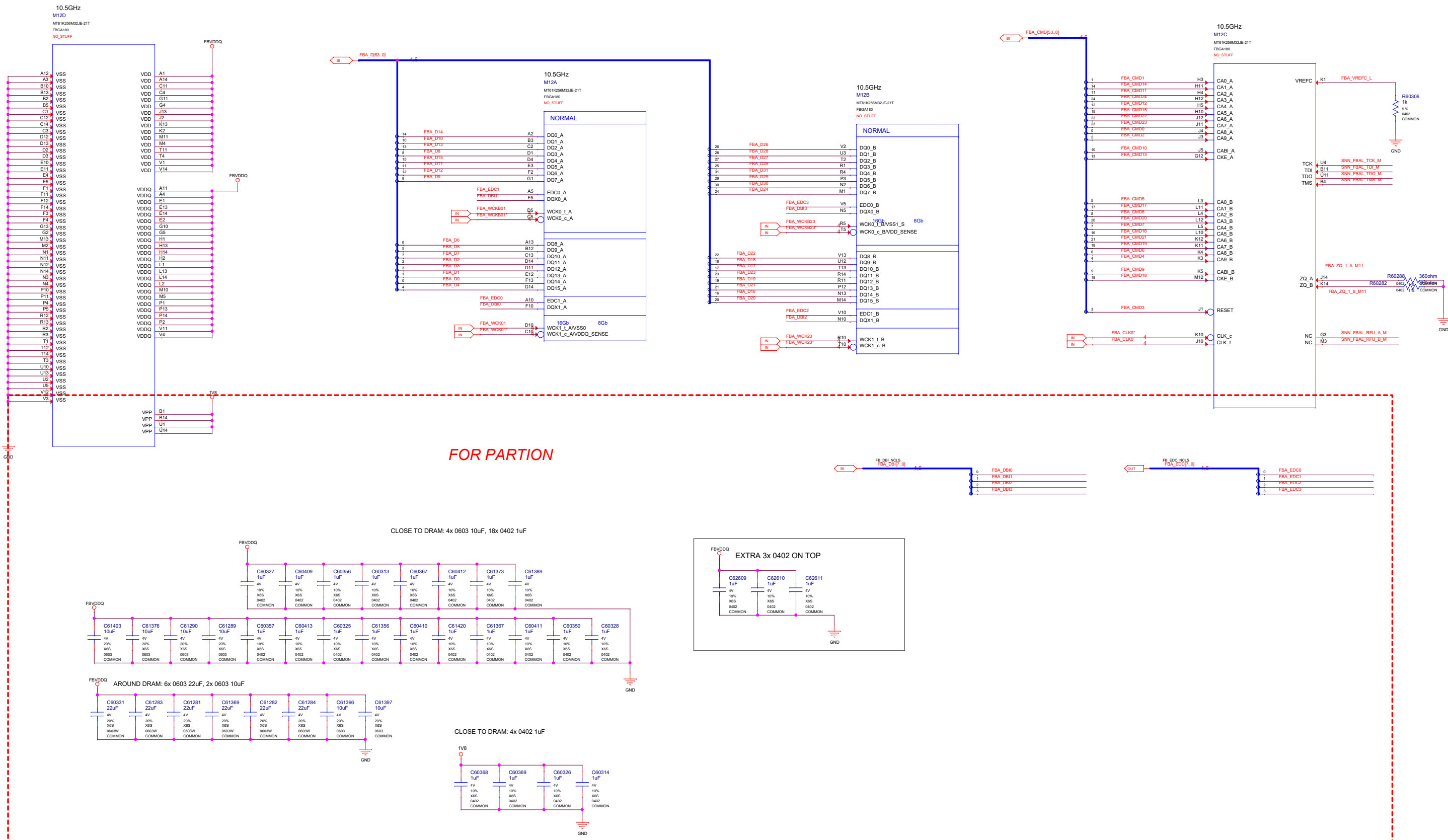
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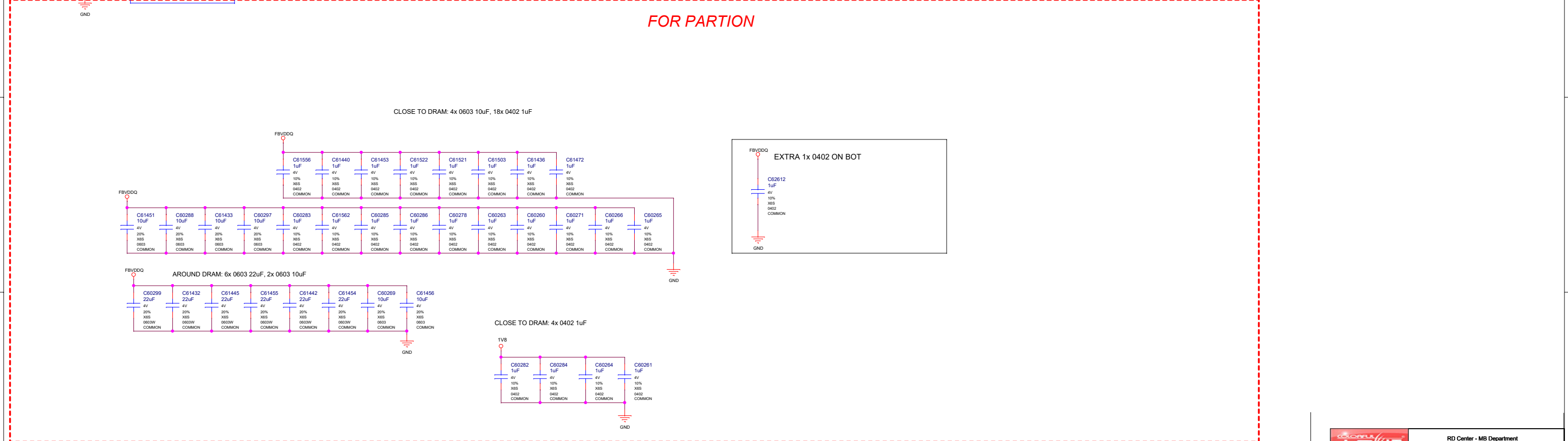
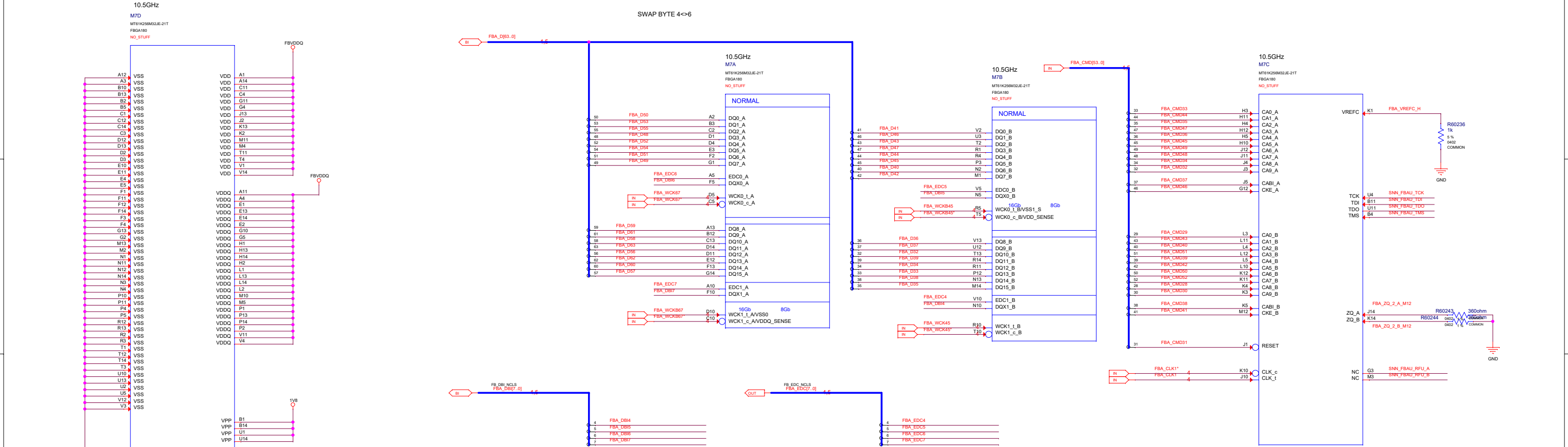
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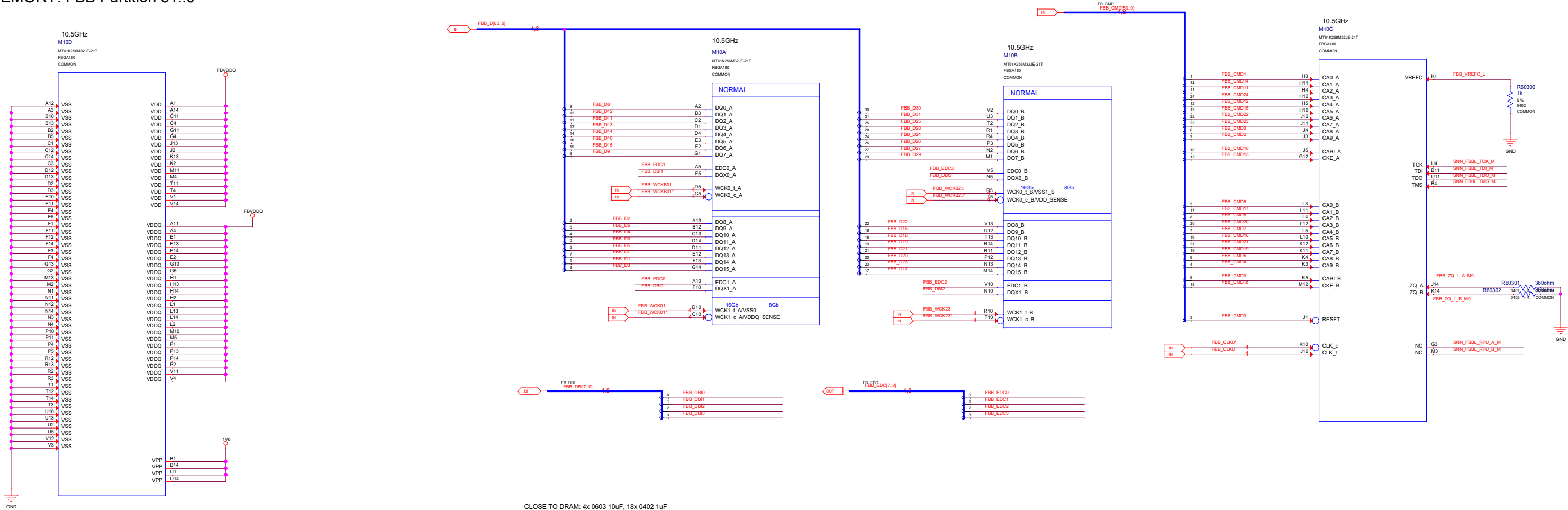
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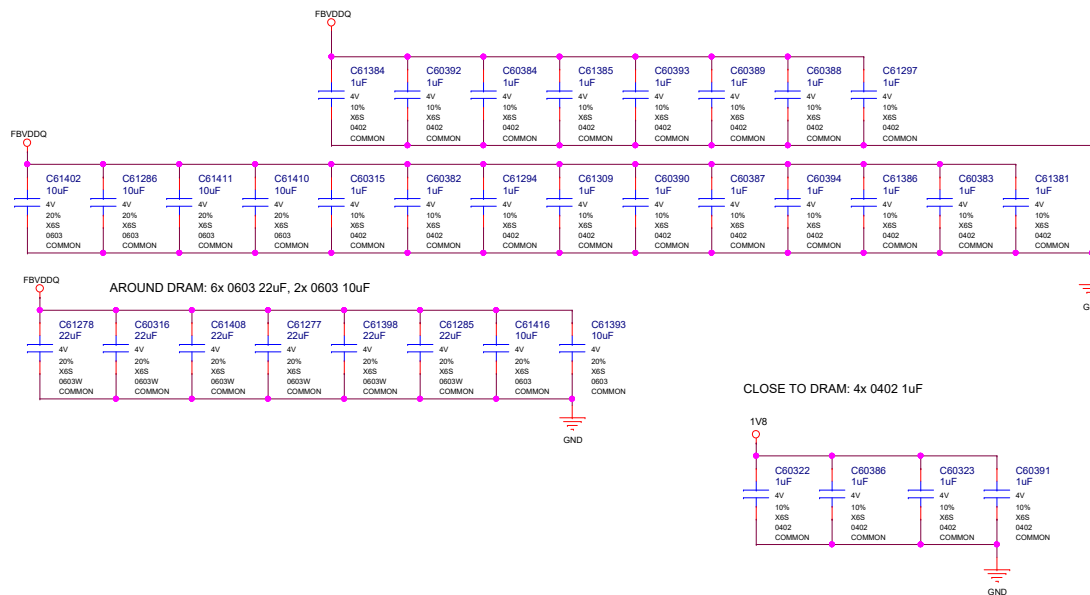
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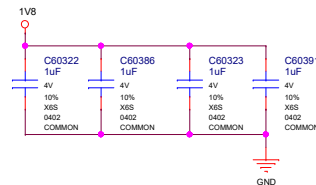
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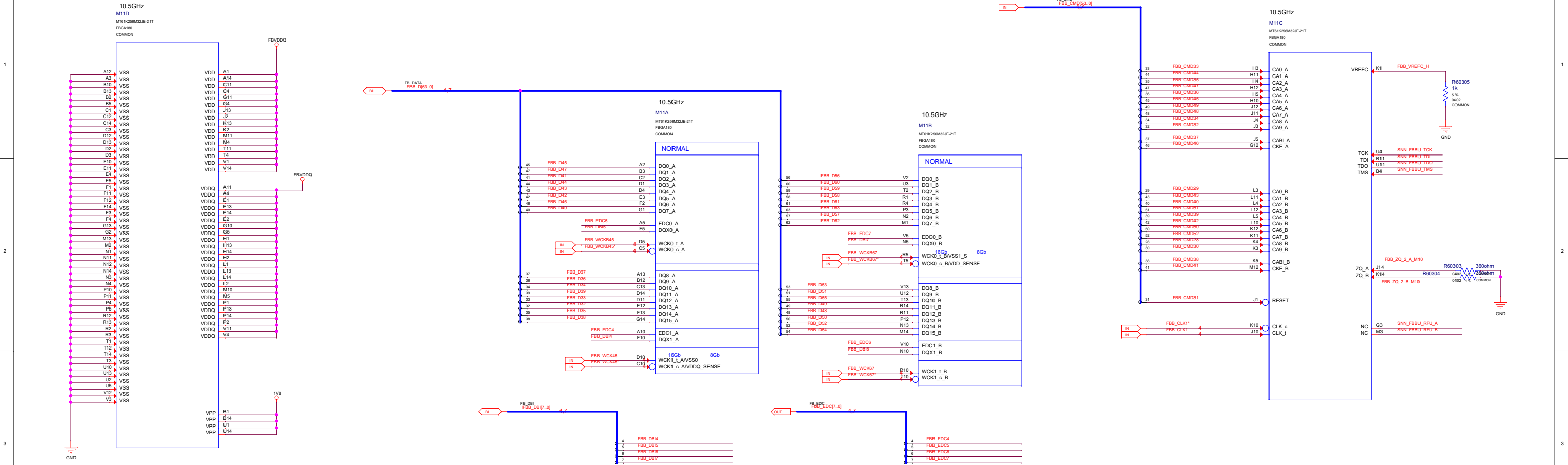
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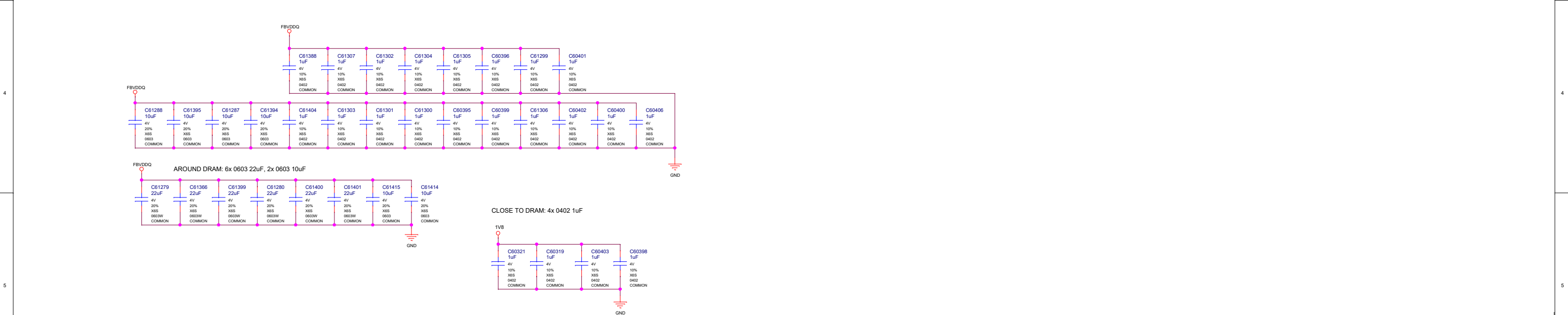
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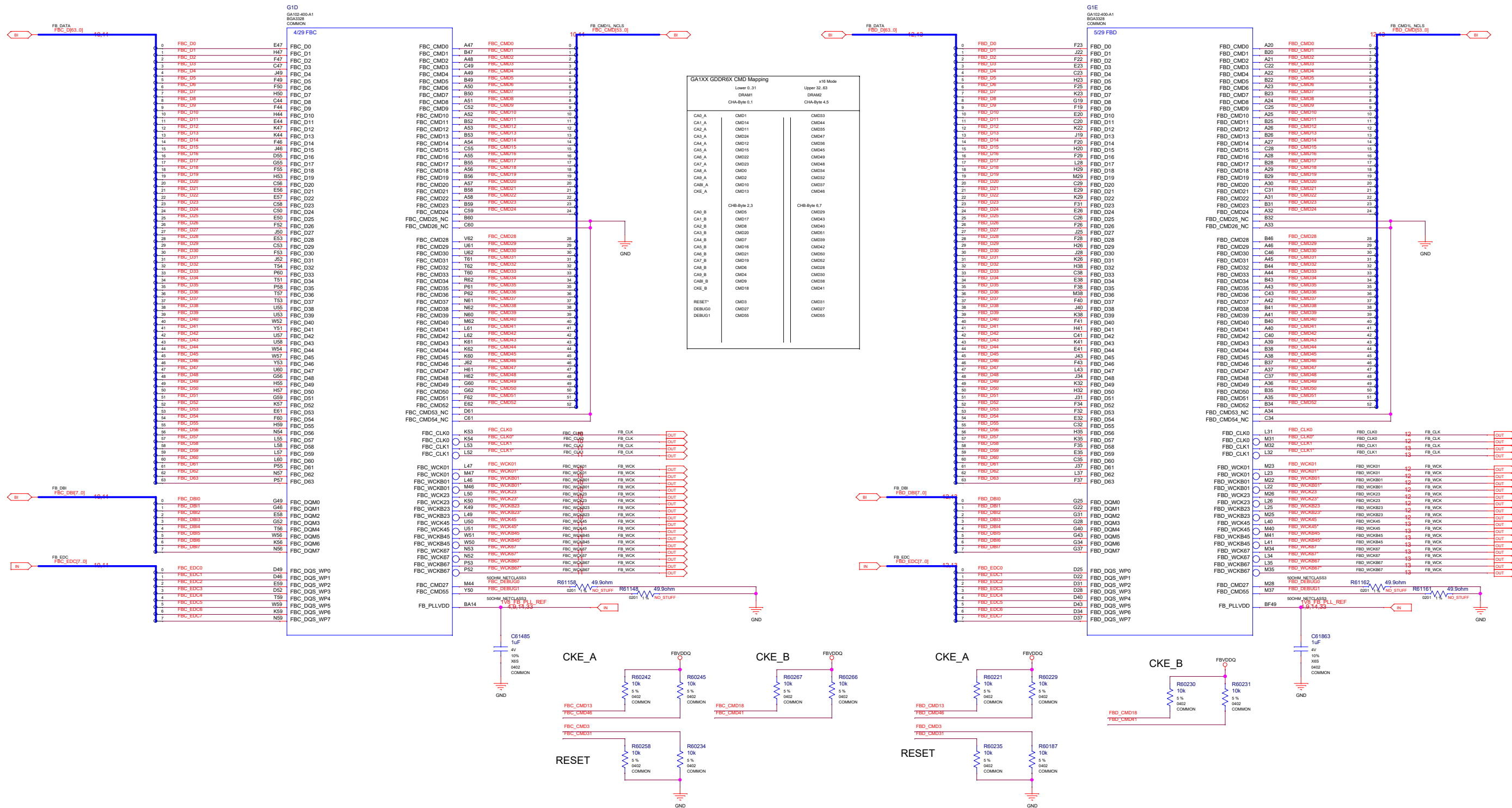


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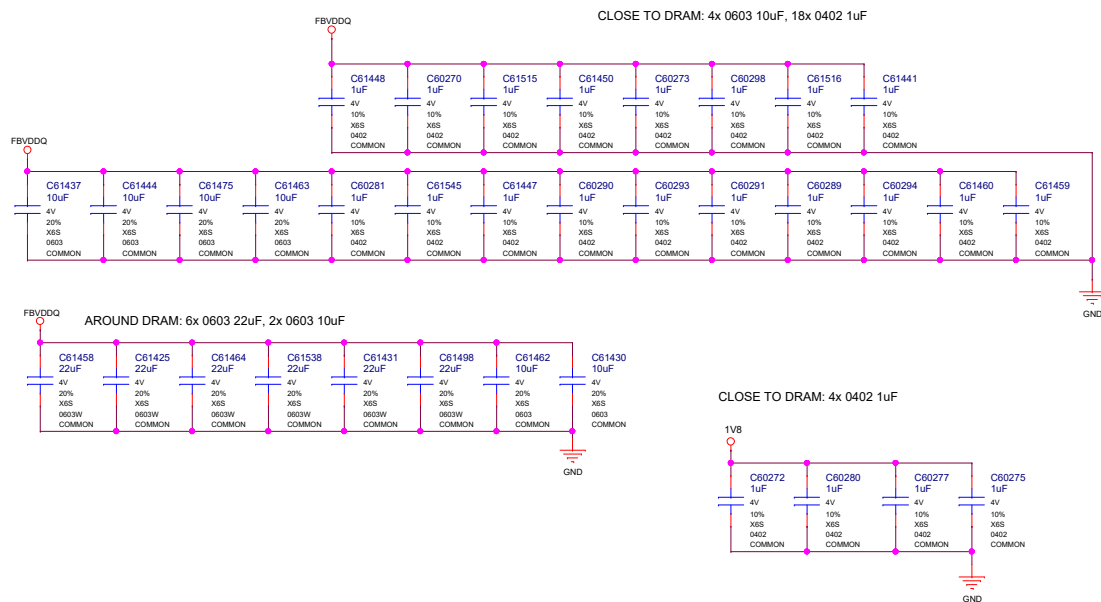
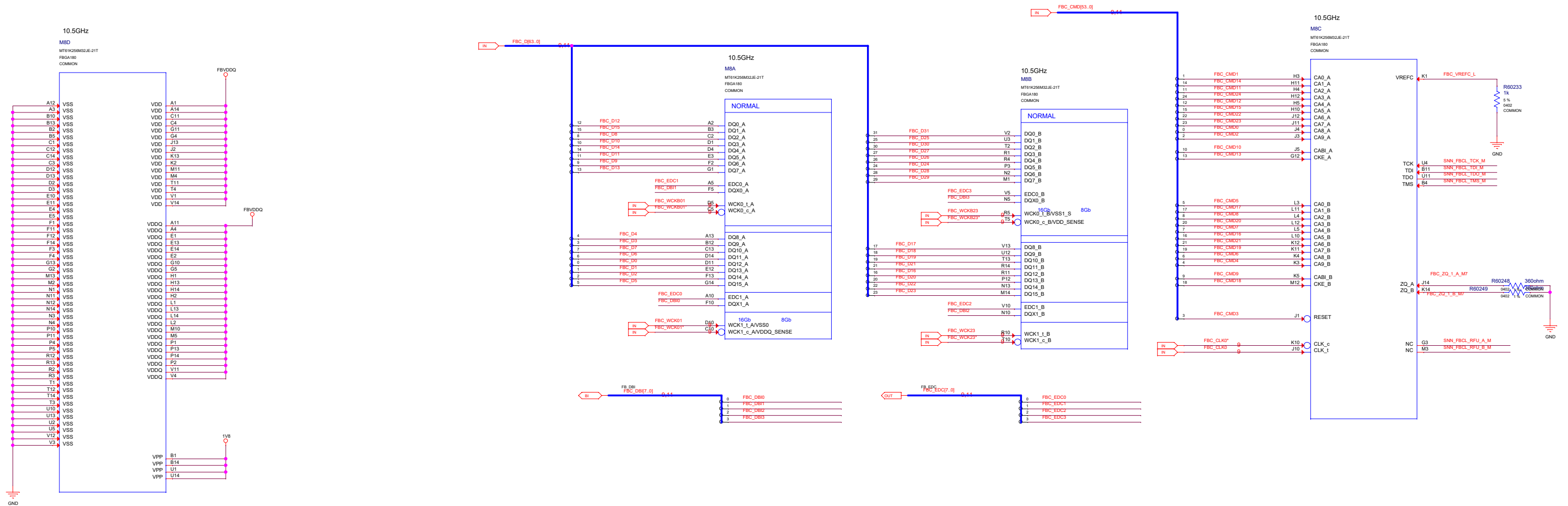


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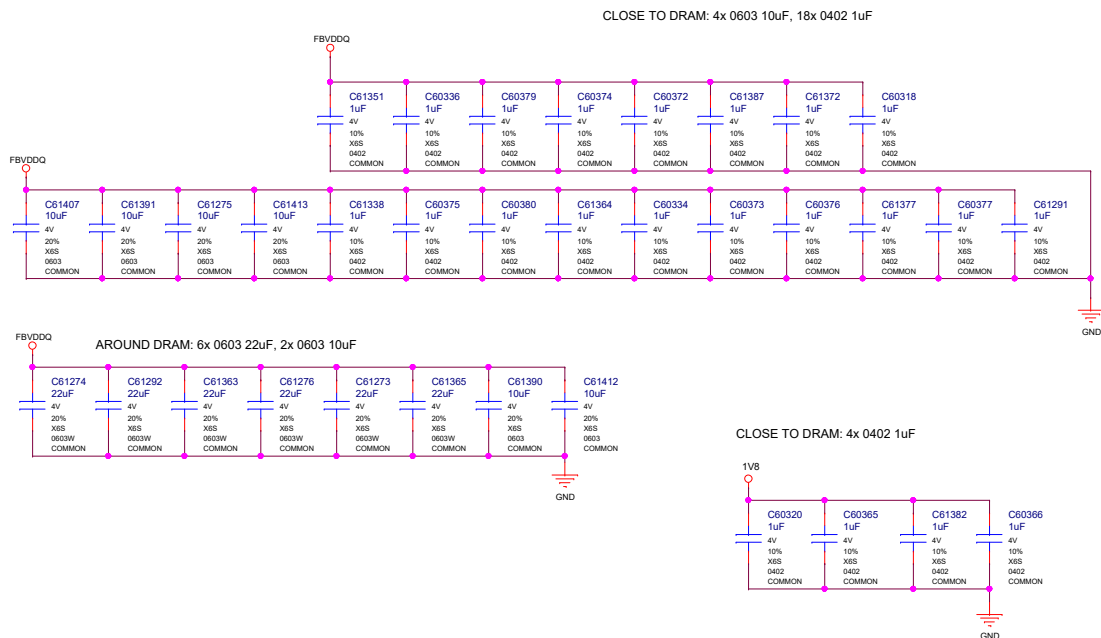
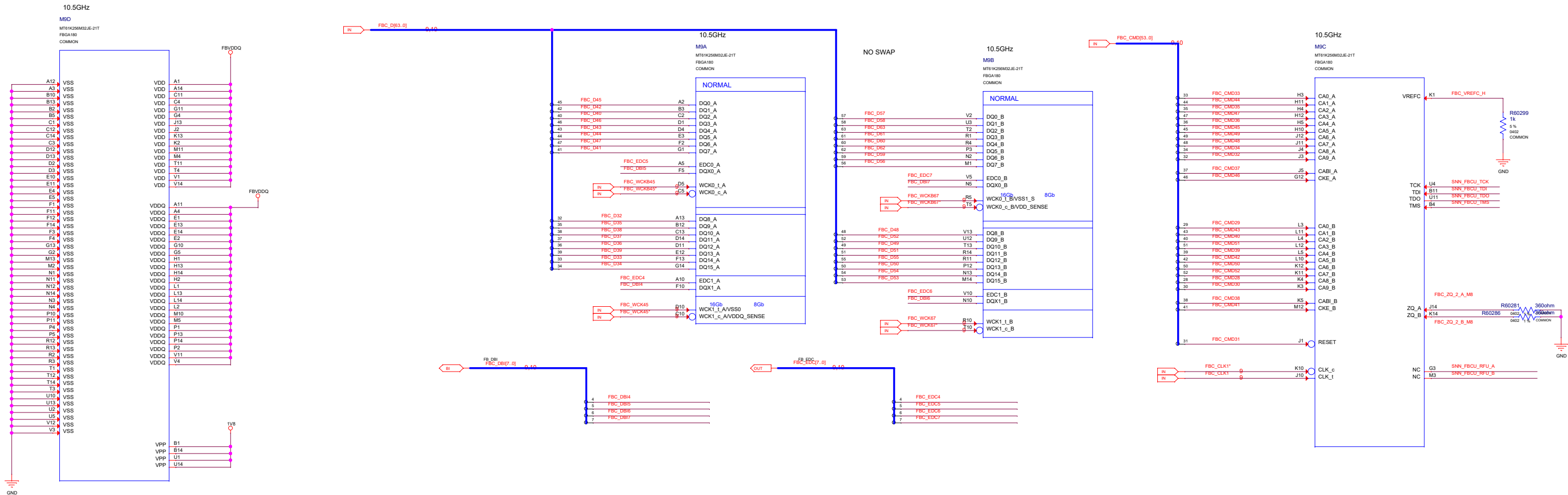
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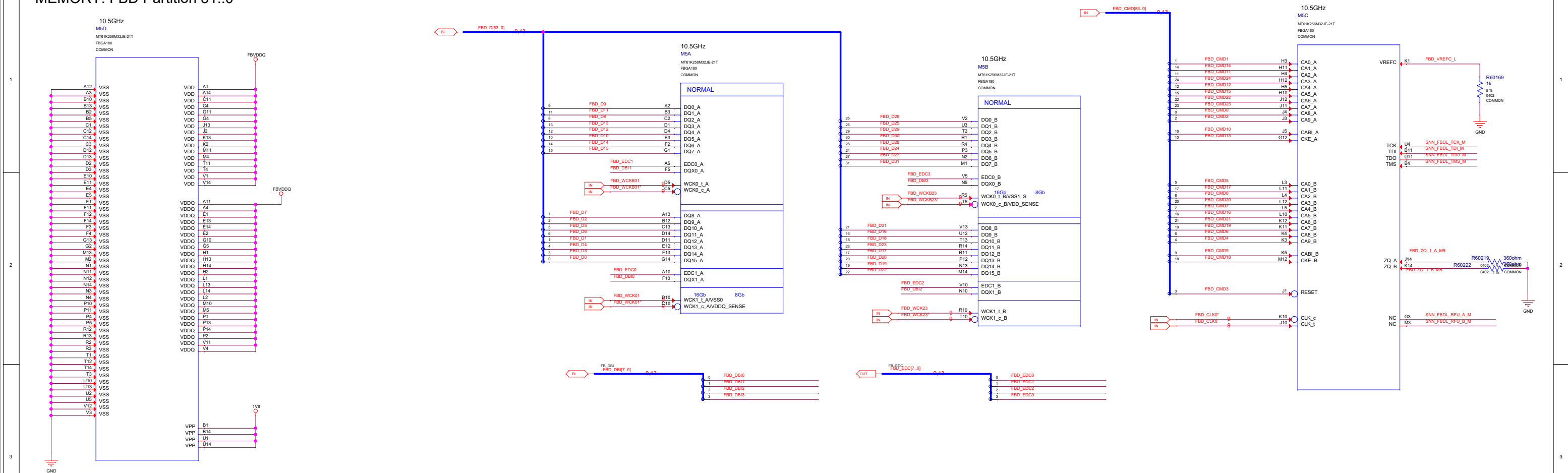
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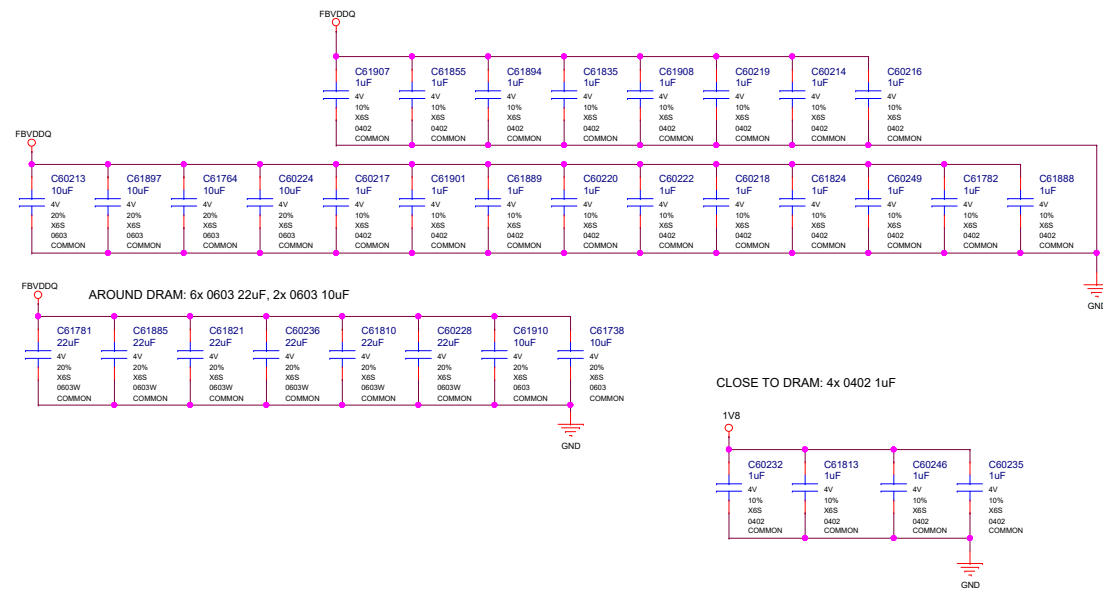
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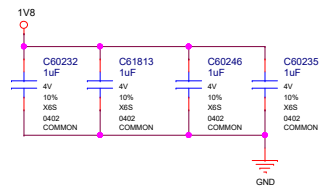
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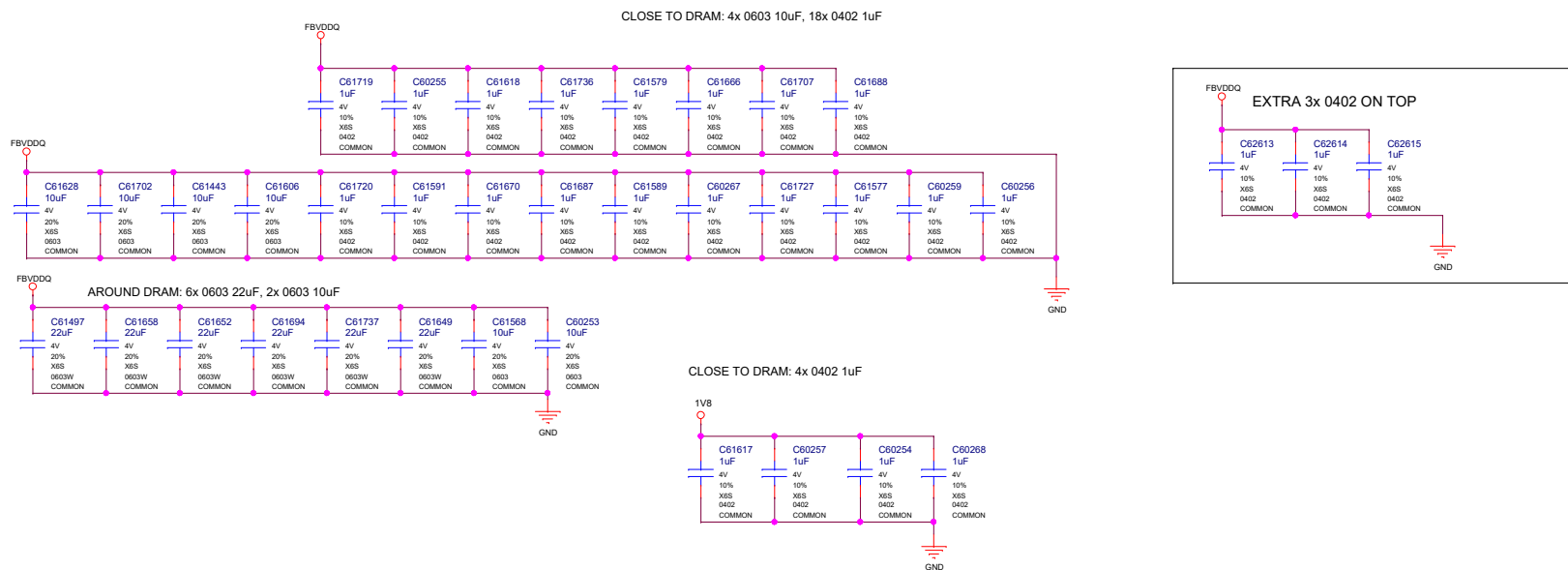
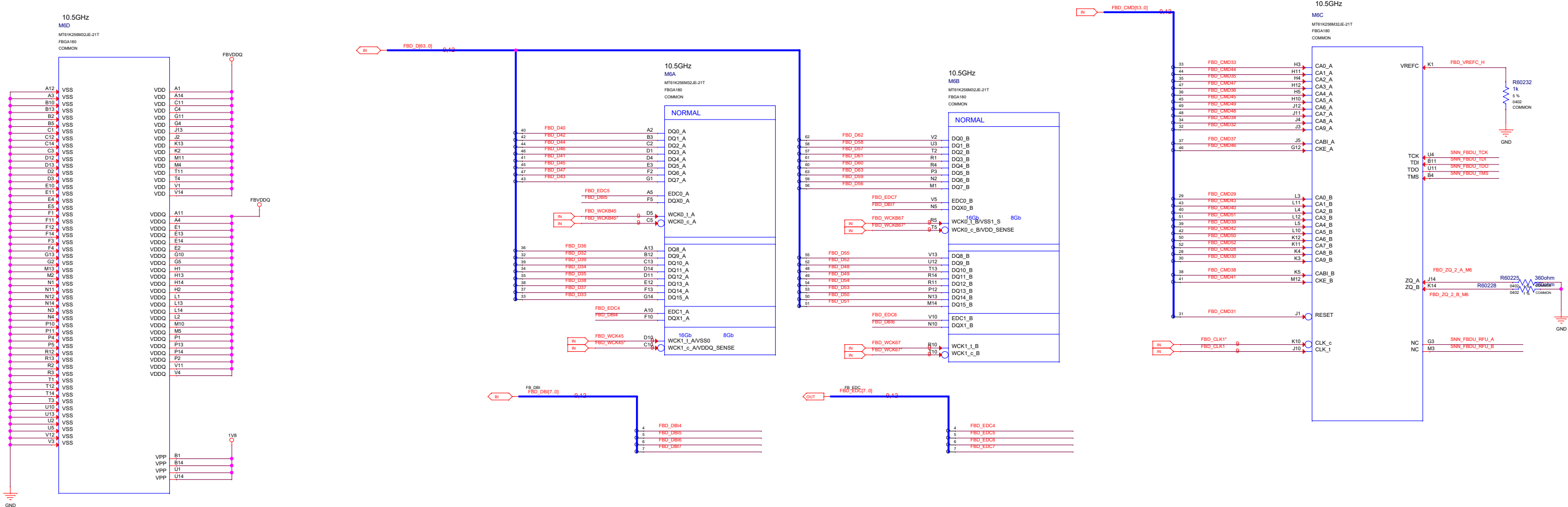
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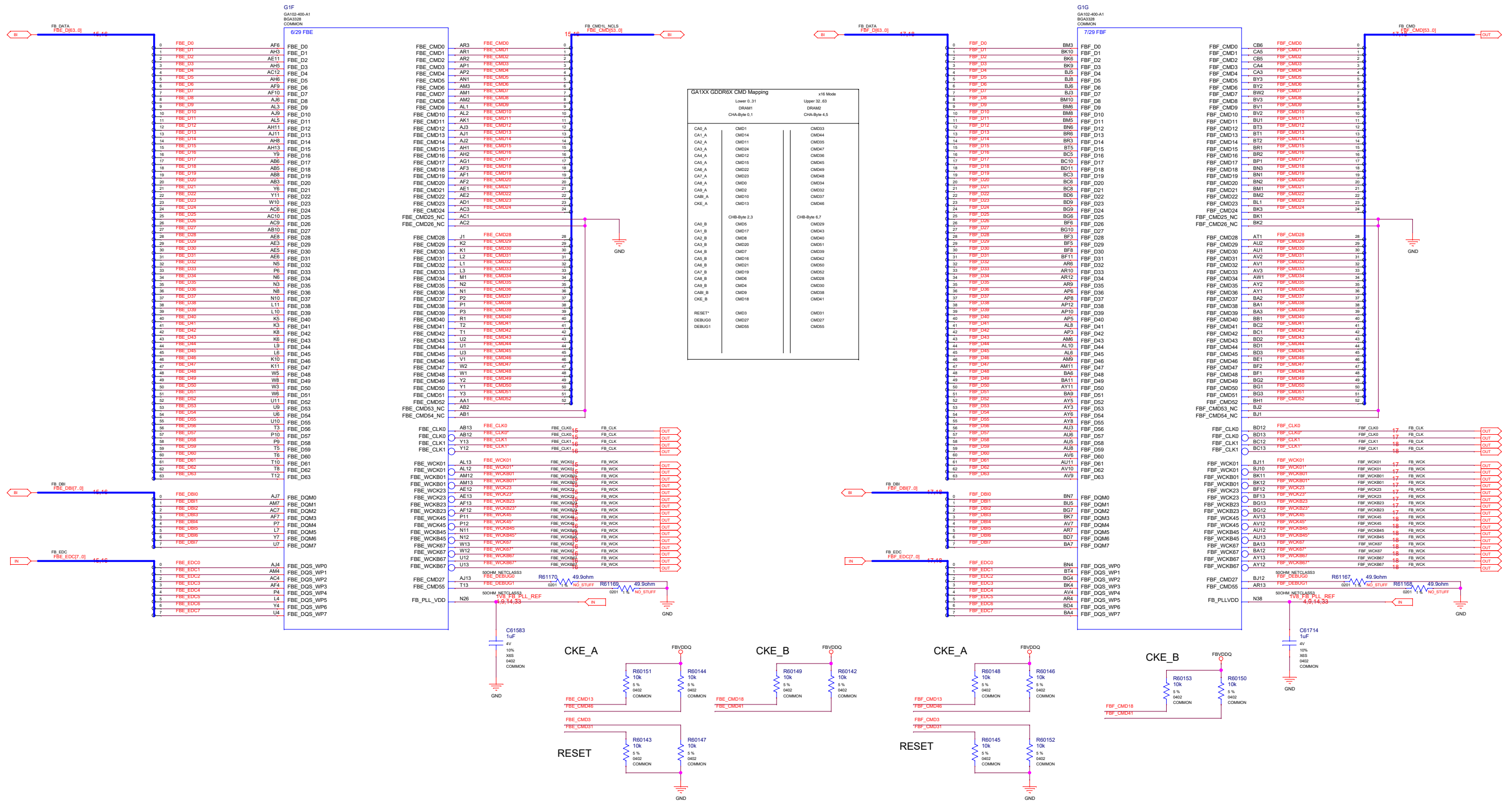
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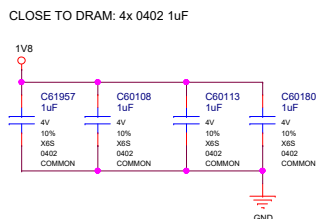
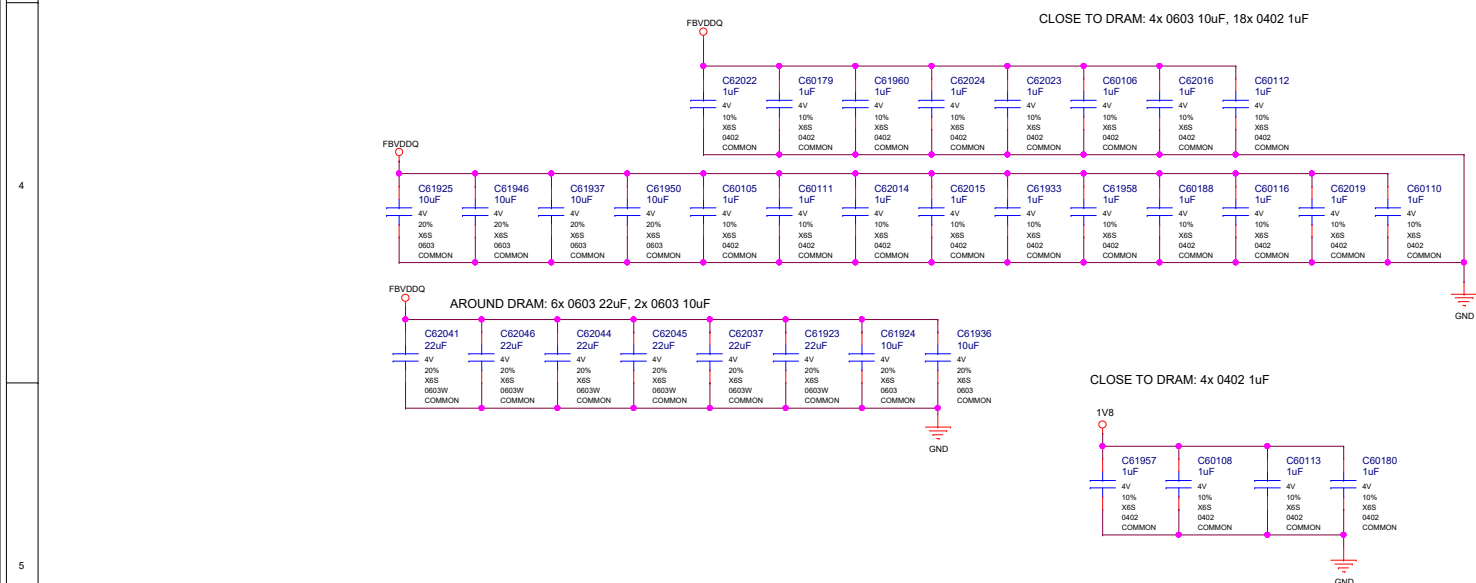
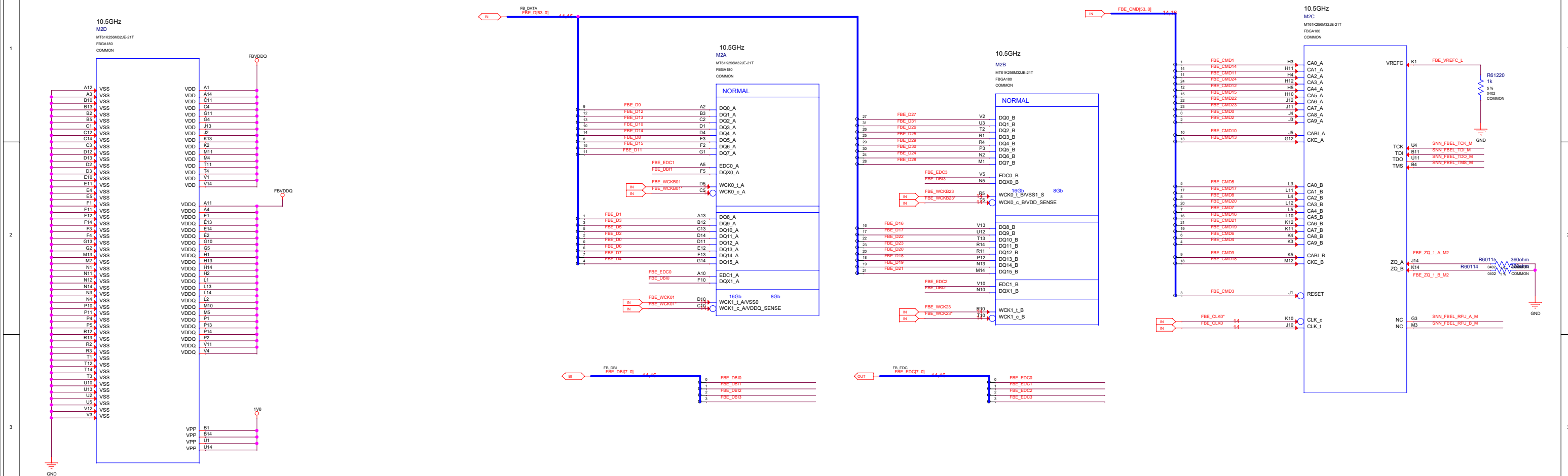
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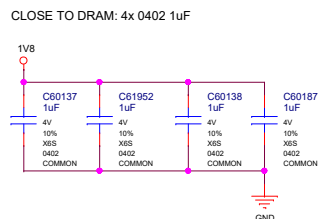
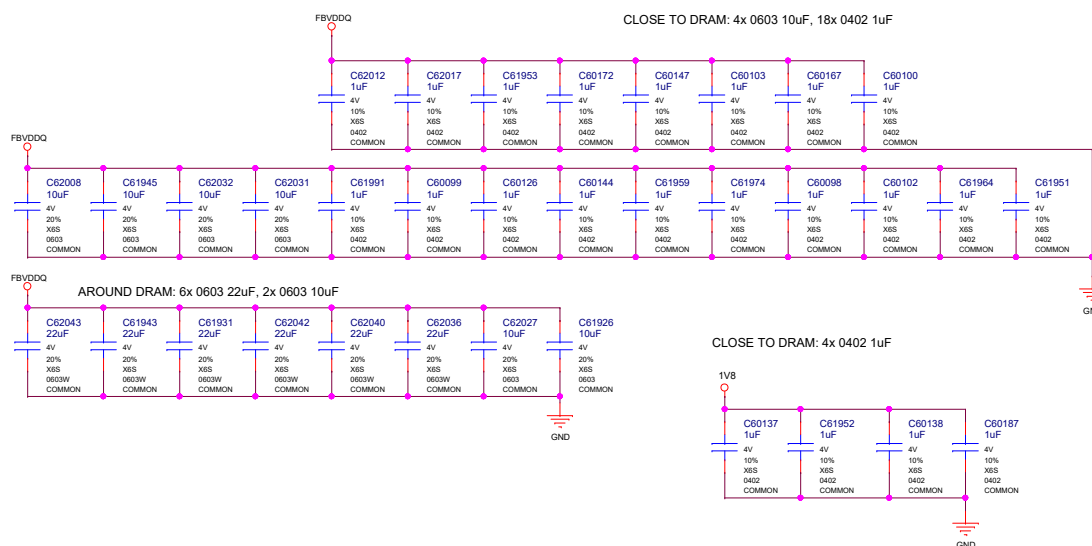
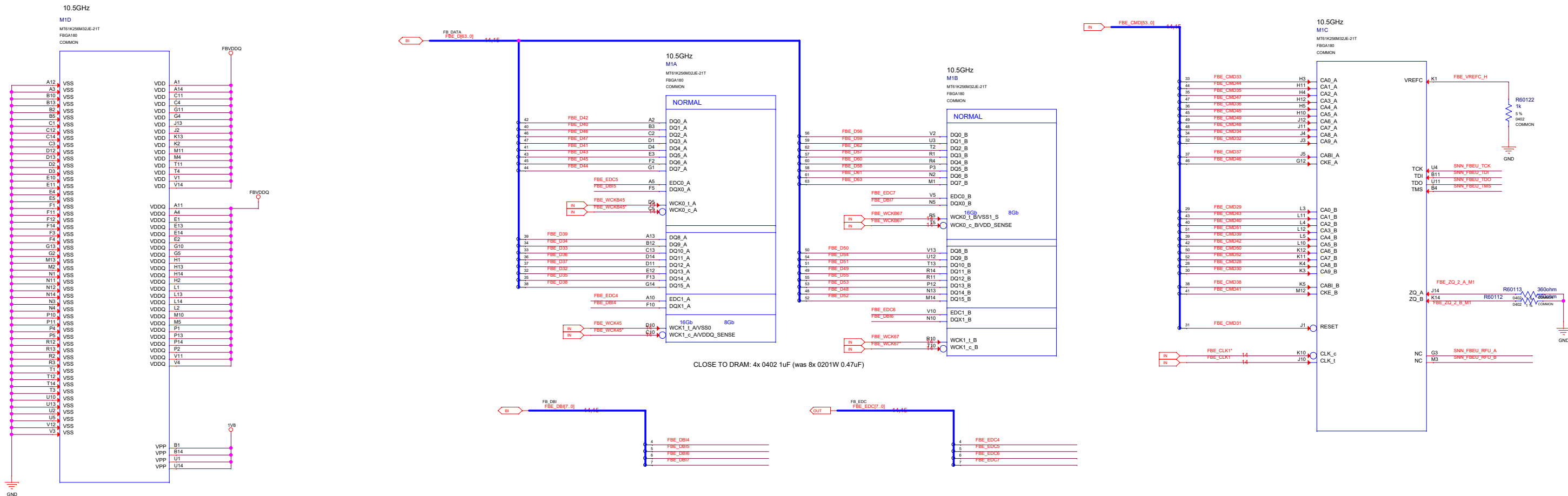
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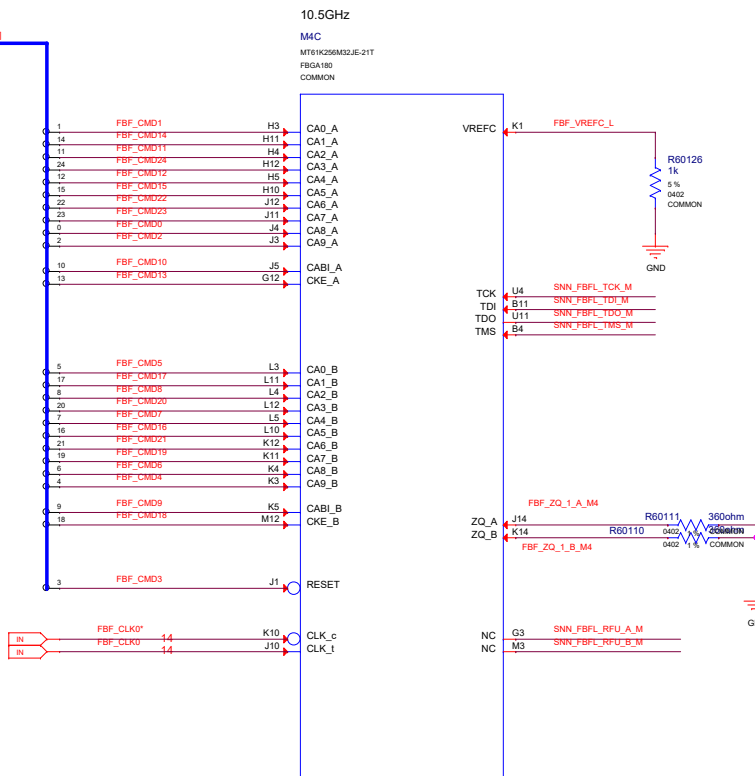
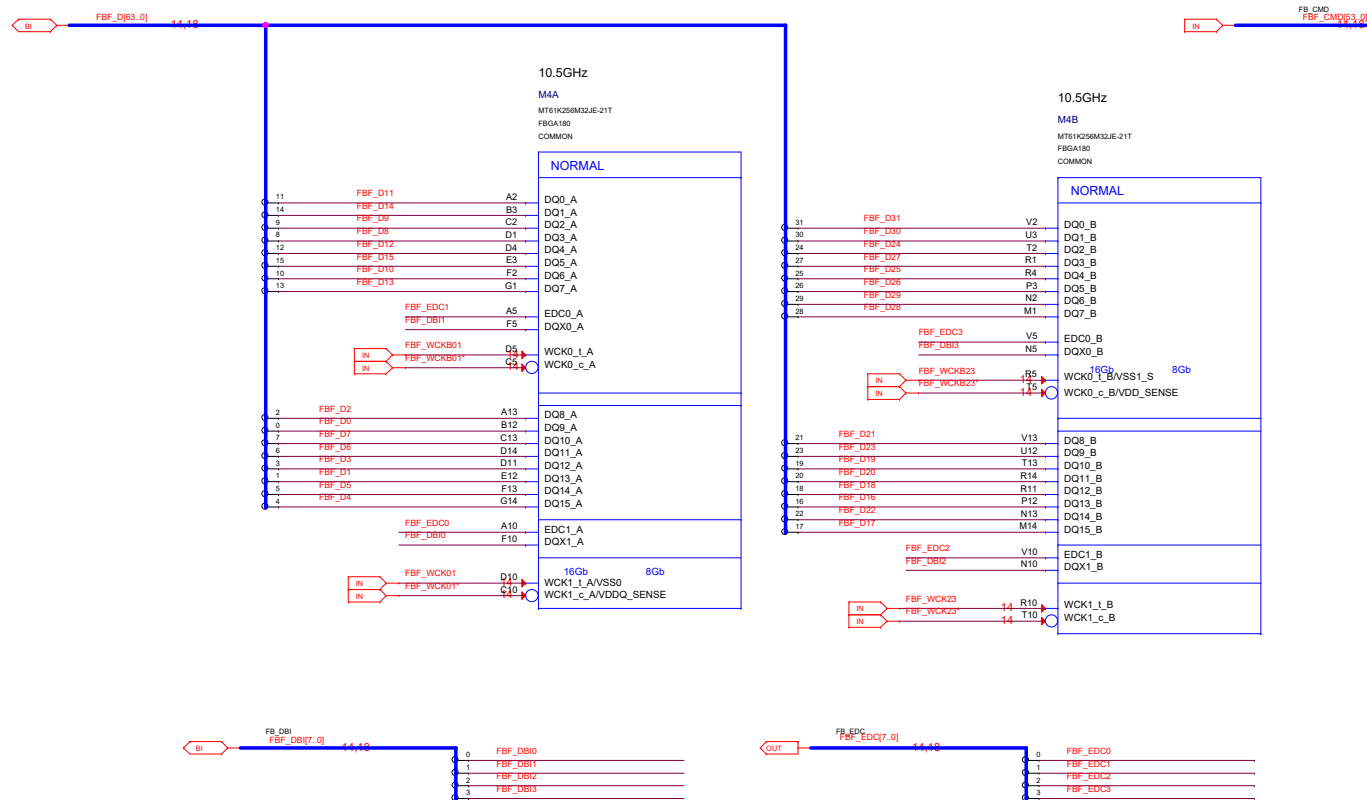
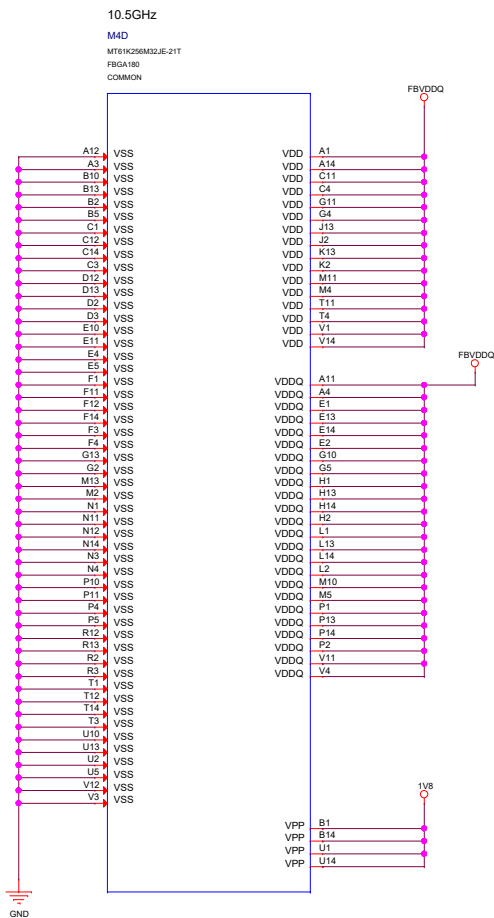
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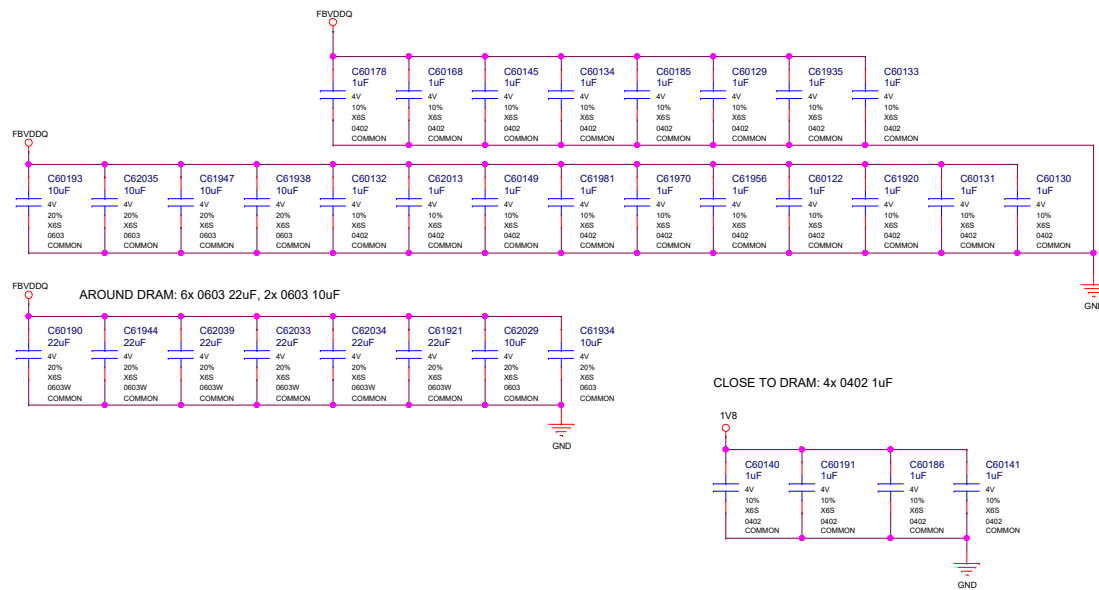
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MEMORY: FBF Partition 31..0

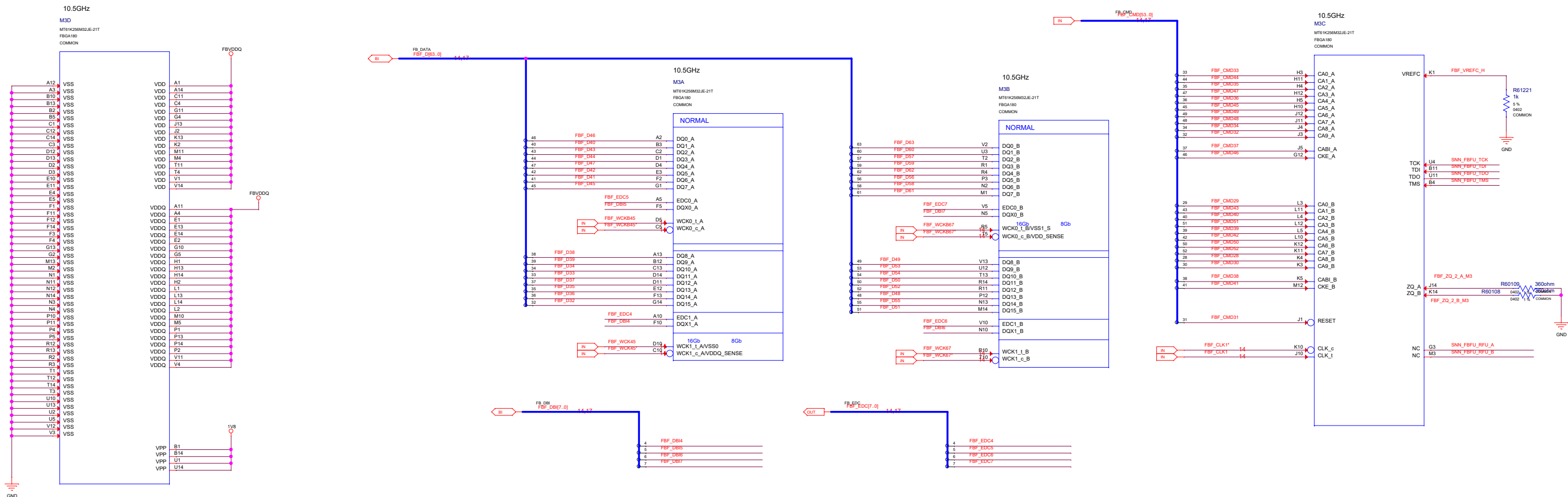


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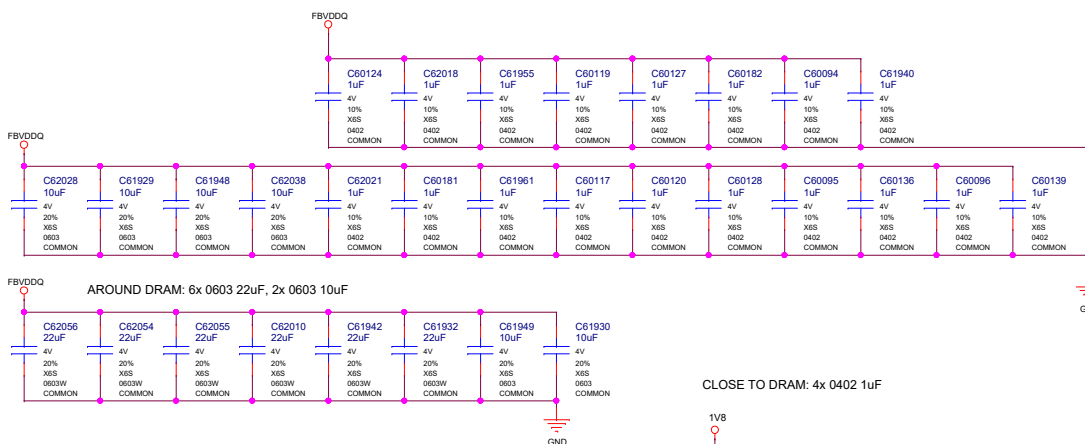


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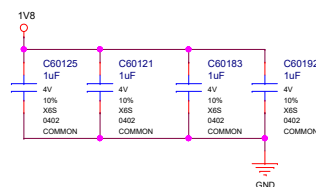
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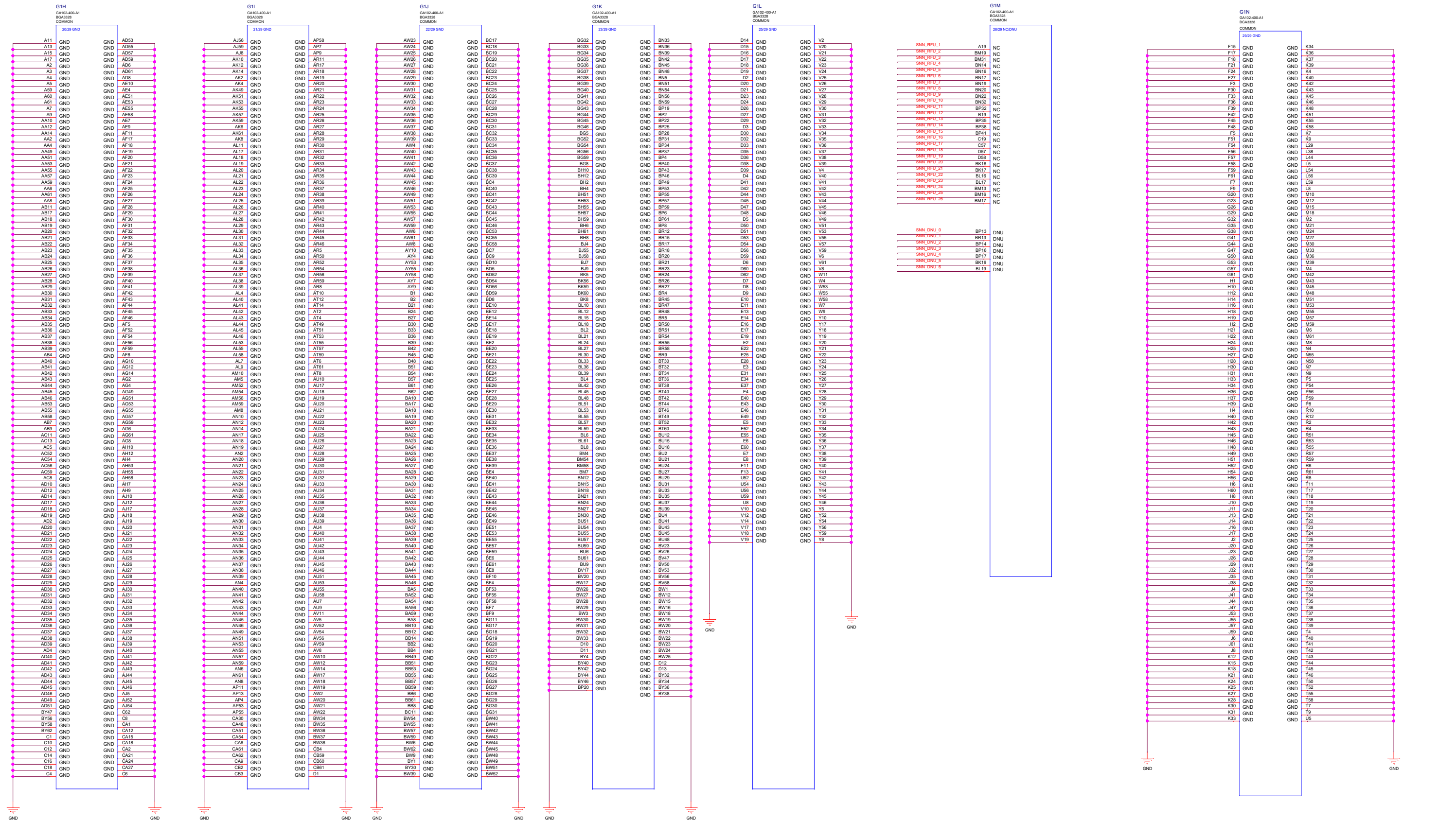
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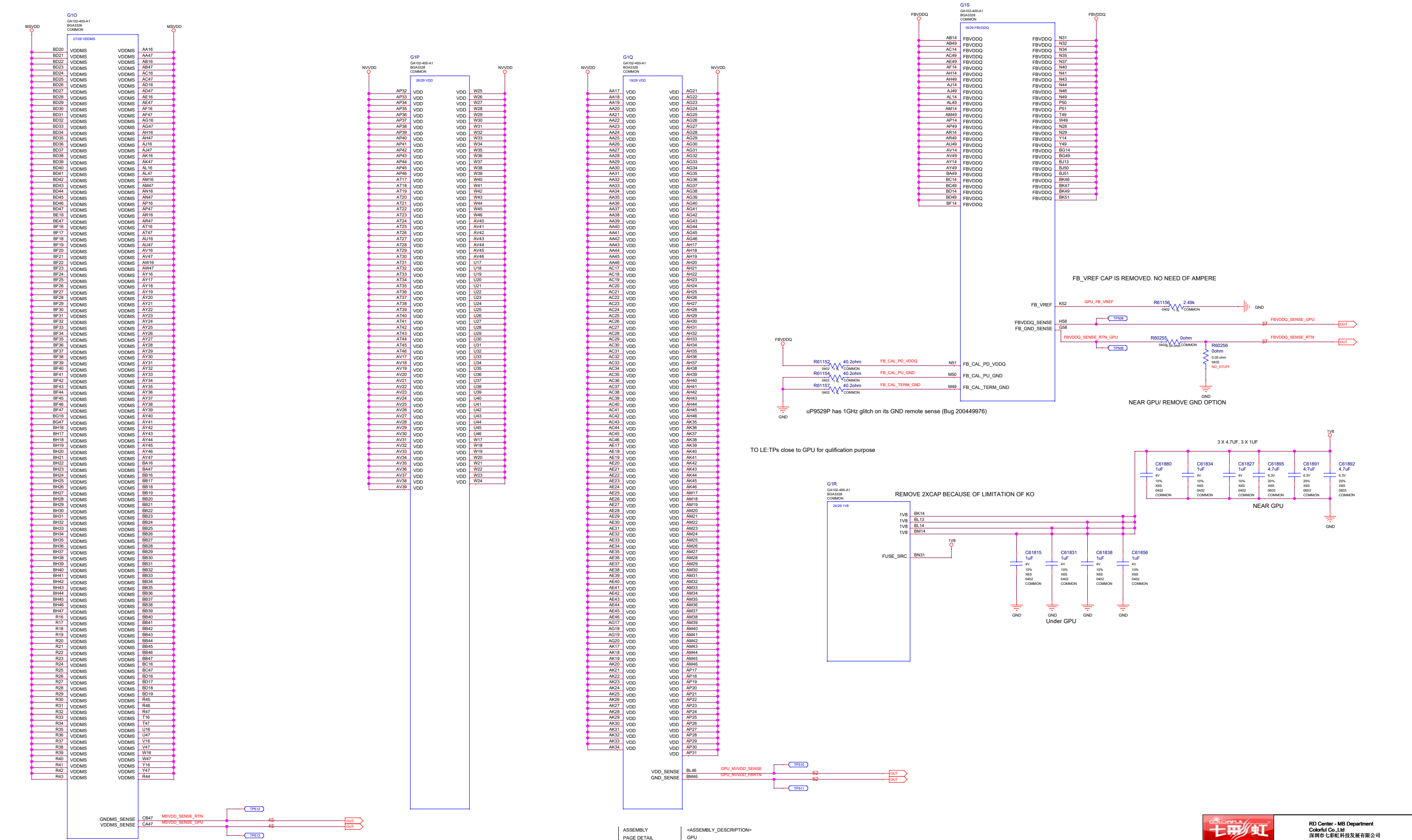
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GPU GND, RFUs & RSVD



GPU PWR and GND

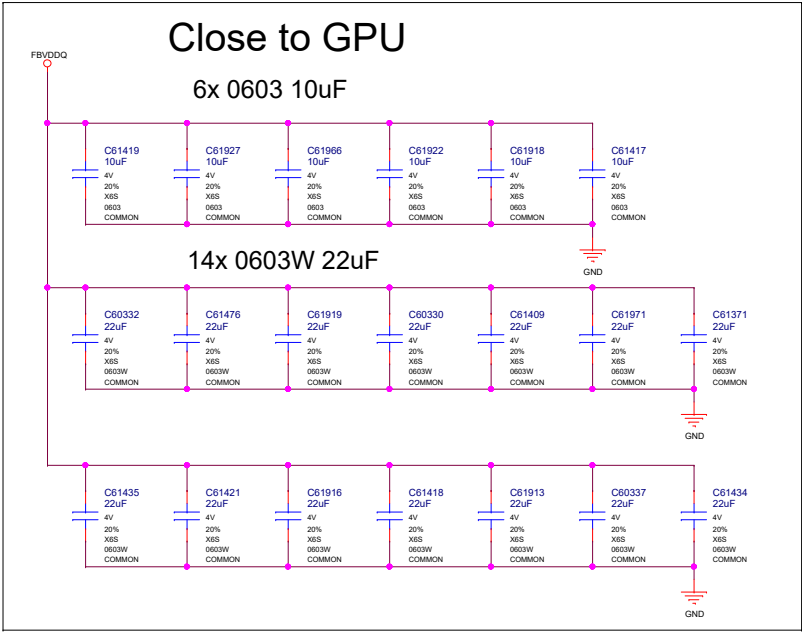
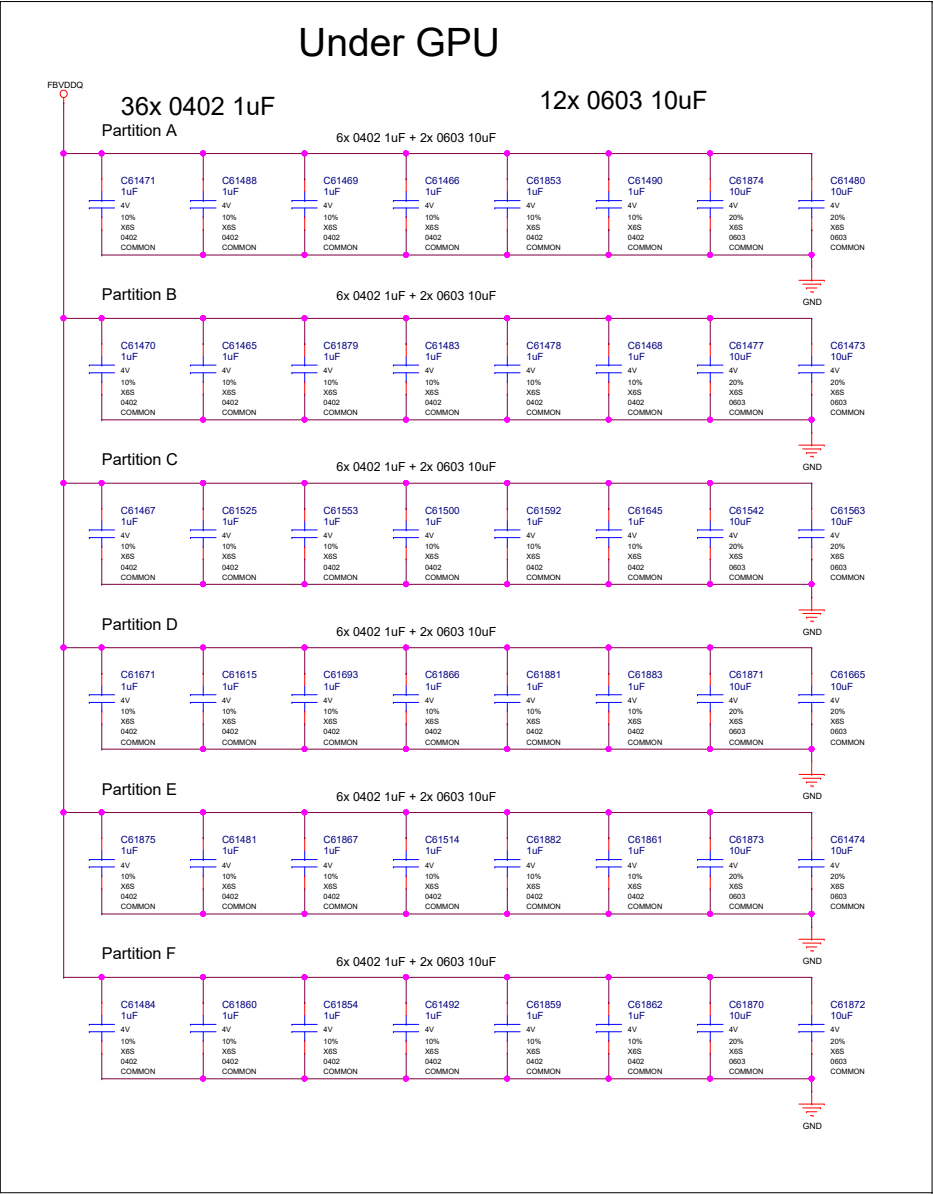


NVVDD UNDER GPU



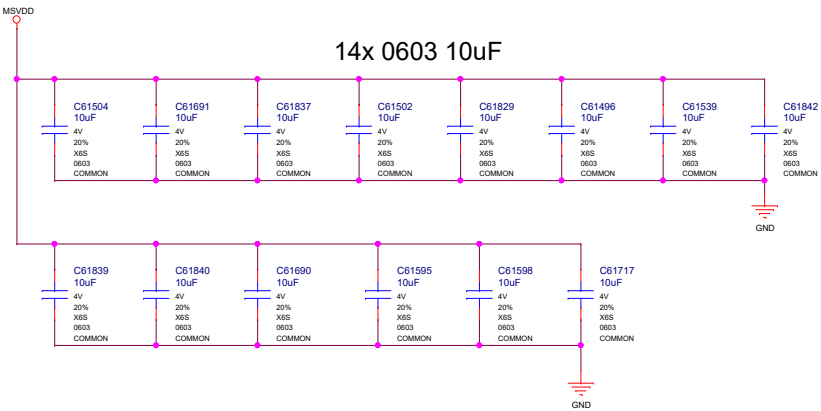
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FBVDDQ

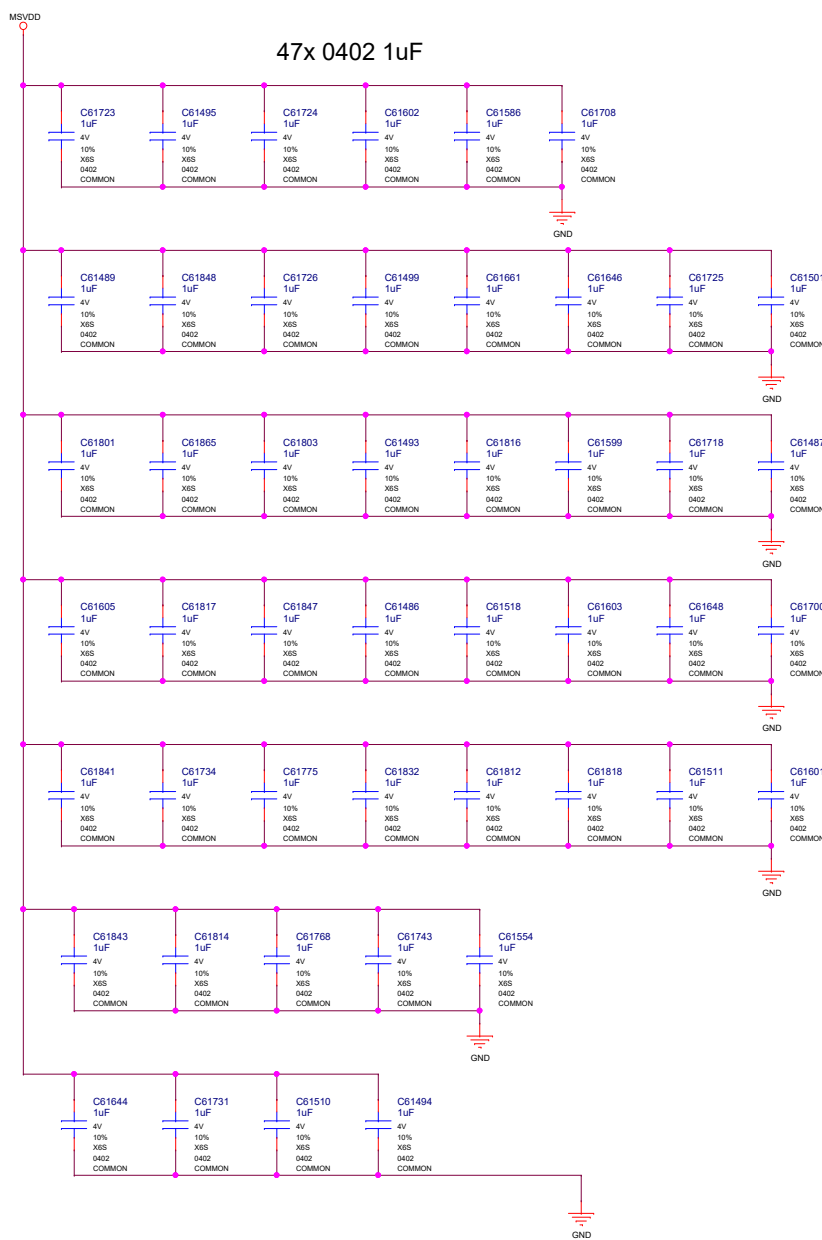
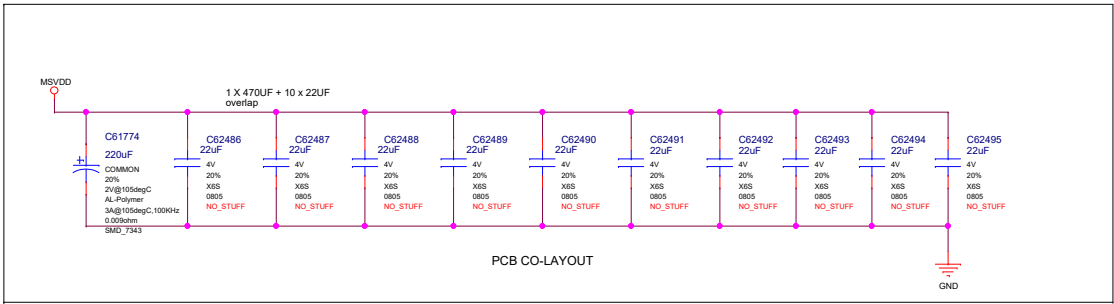
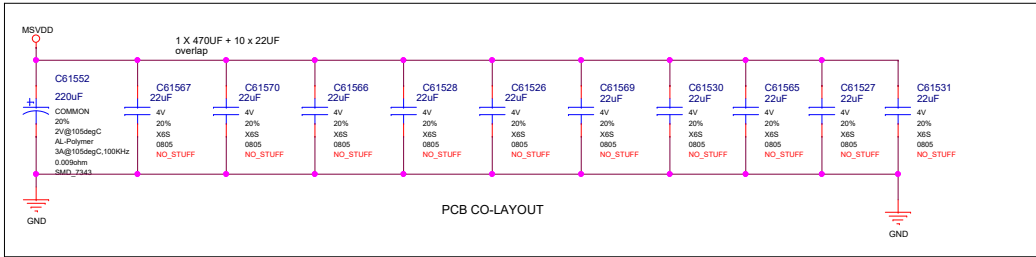


MSVDD

UNDER GPU



2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION




	A	B	C	D	E	F	G	H
1								
2								
3								
4								
5								

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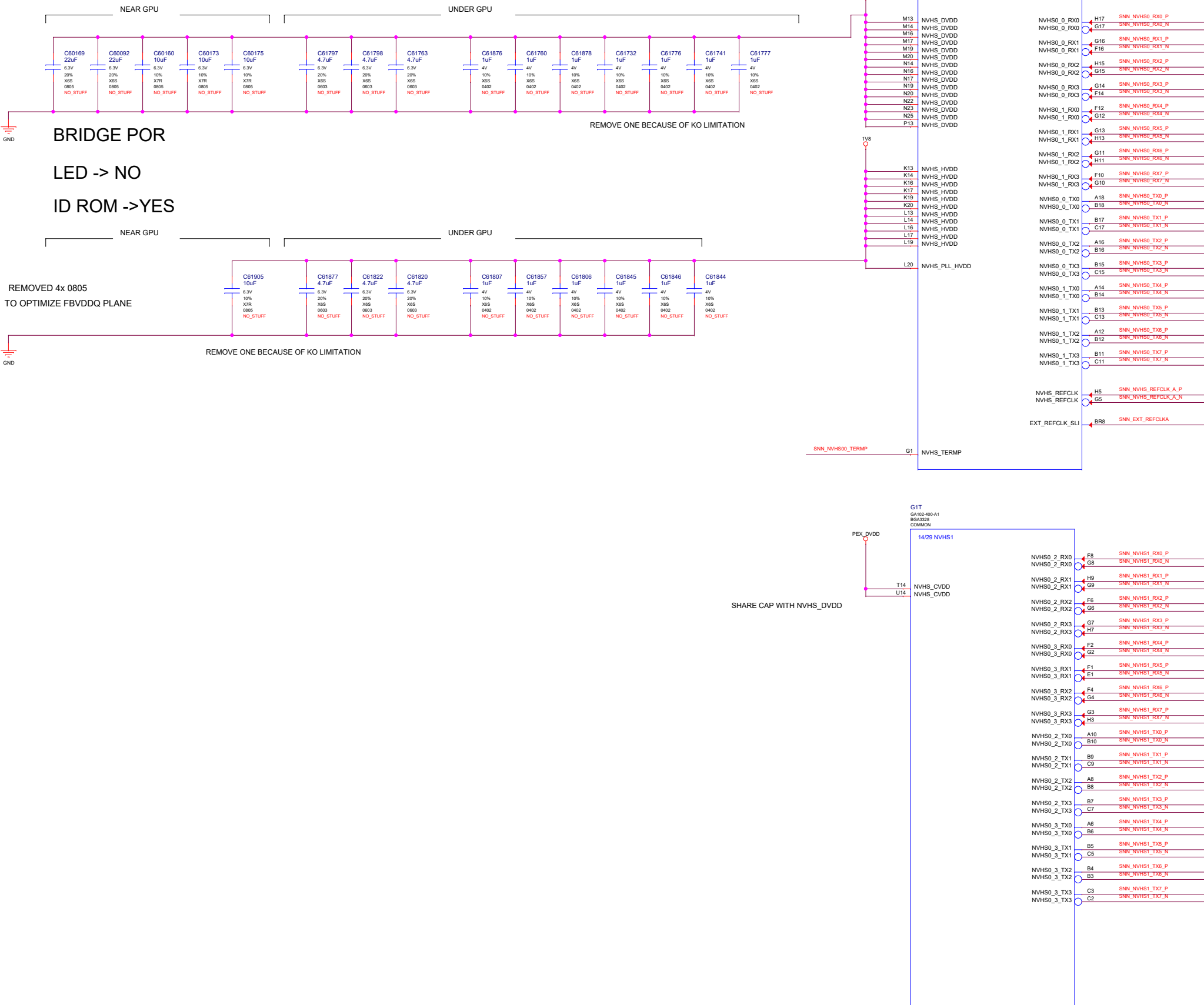
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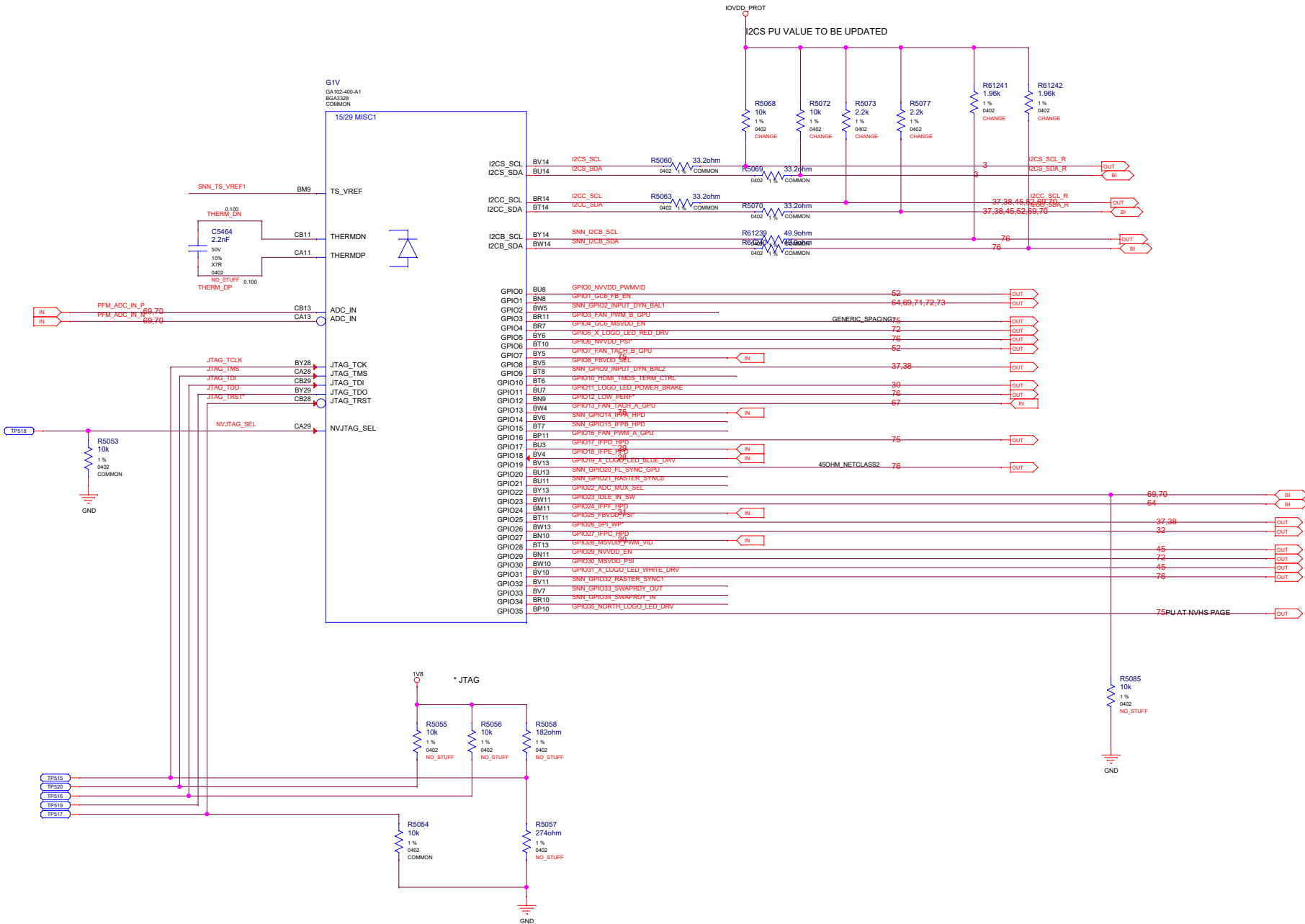
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NVHS Interface and FRAME LOCK



MISC1: Fan, Thermal, JTAG, GPIO, STEREO

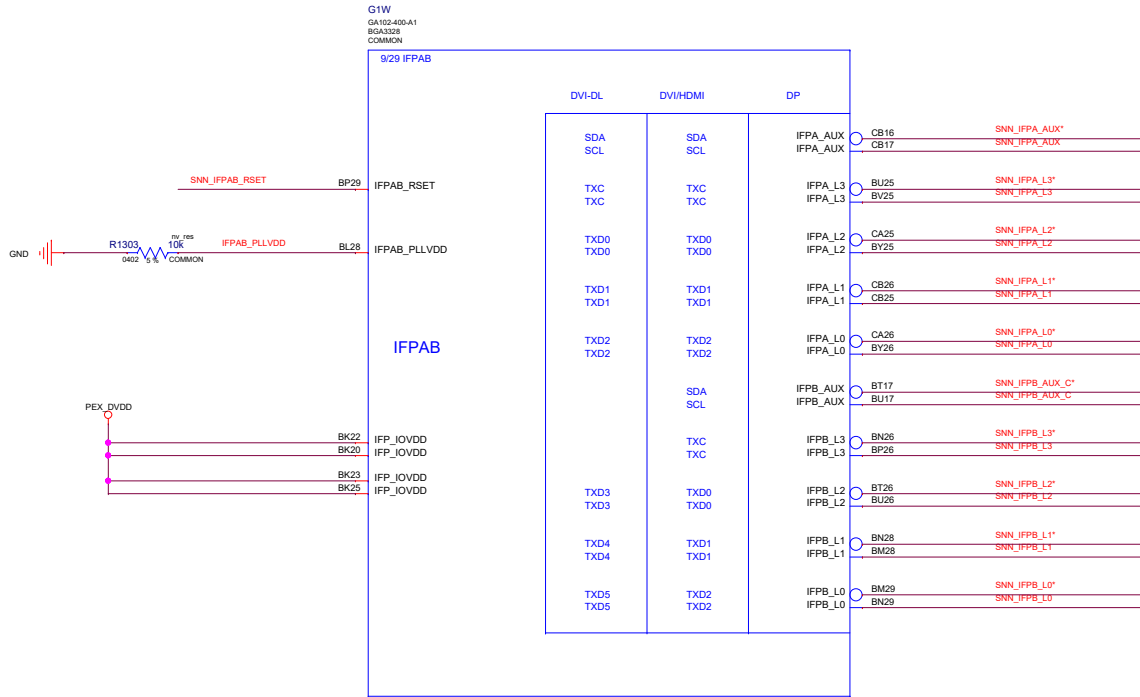


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ASSEMBLY
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MISC: THERMAL, JTAG, GPIO

IFPA UNUSED, IFPB UNUSED



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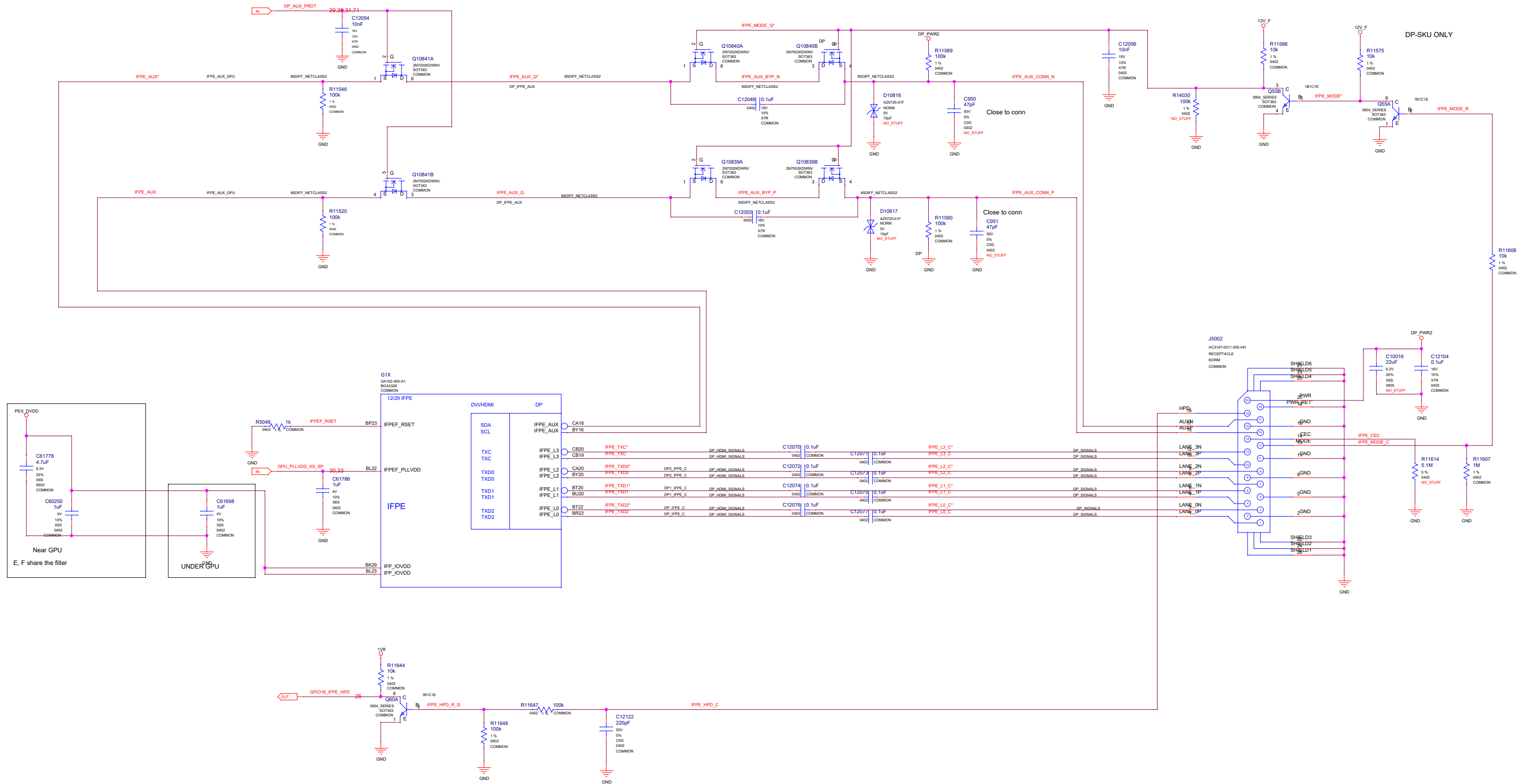
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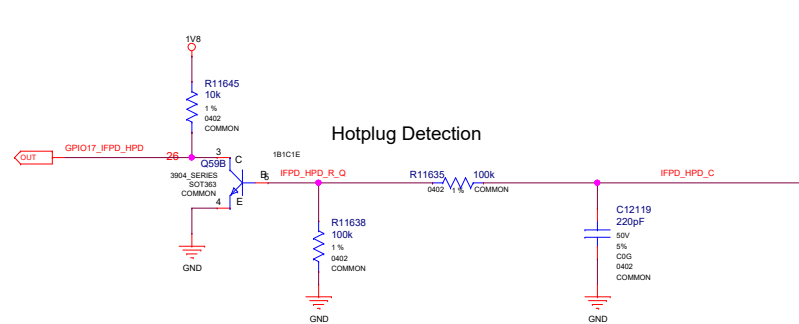
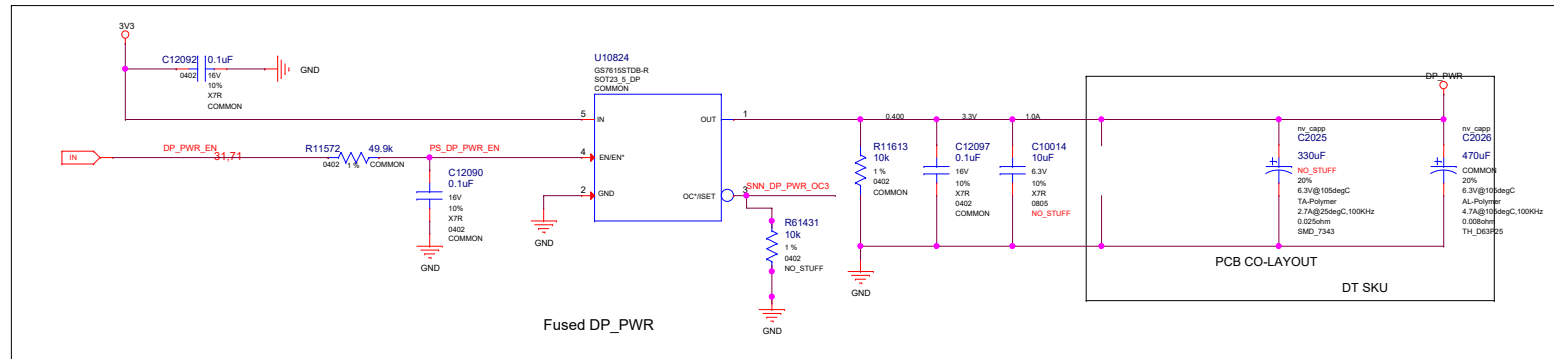
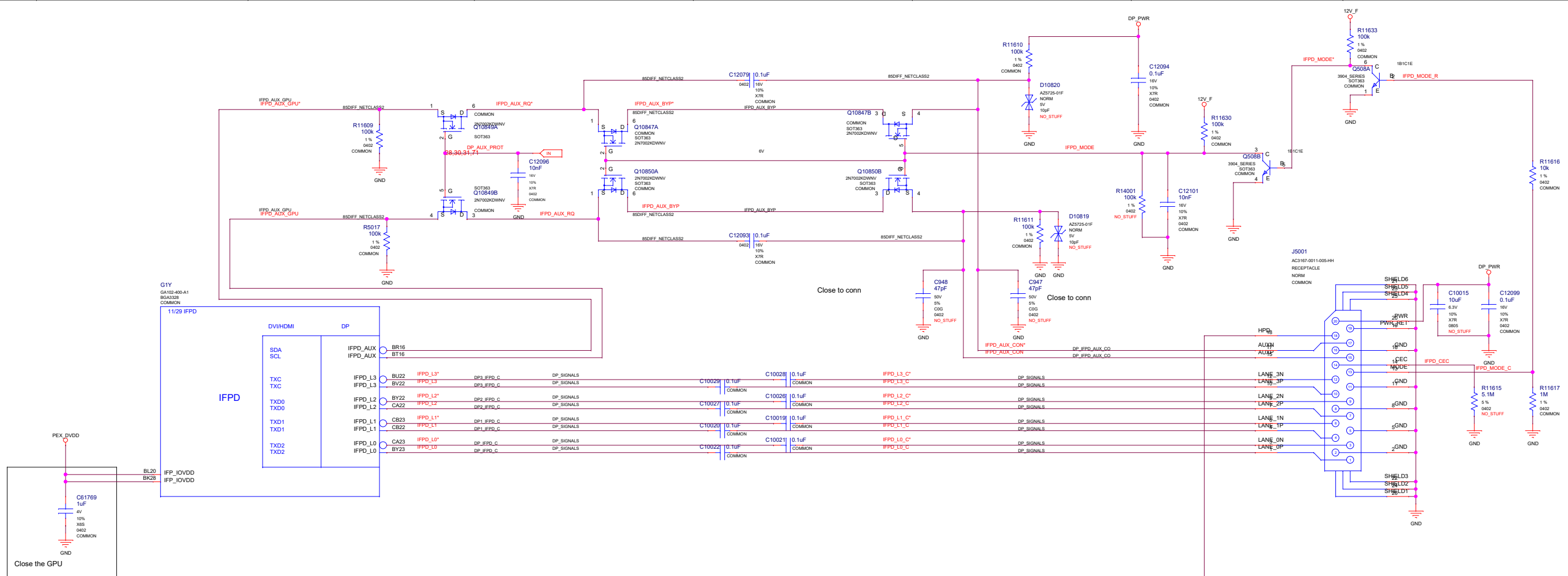
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IFPE DP



IFPD DP



IFPC HDMI/DP

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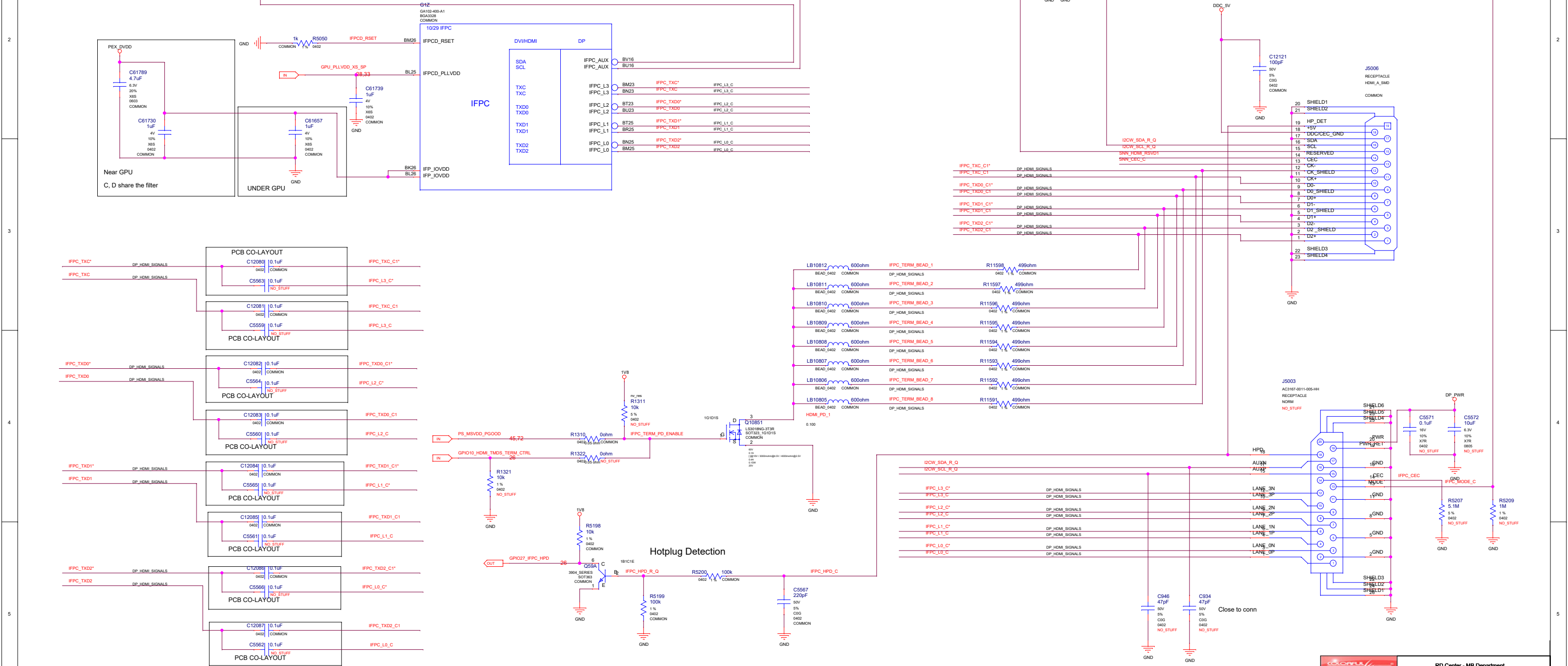
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ASSEMBLY
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IFPC HDMI/DP



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MISC: ROM, Straps

GROUP0				
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

<-A01 PCB

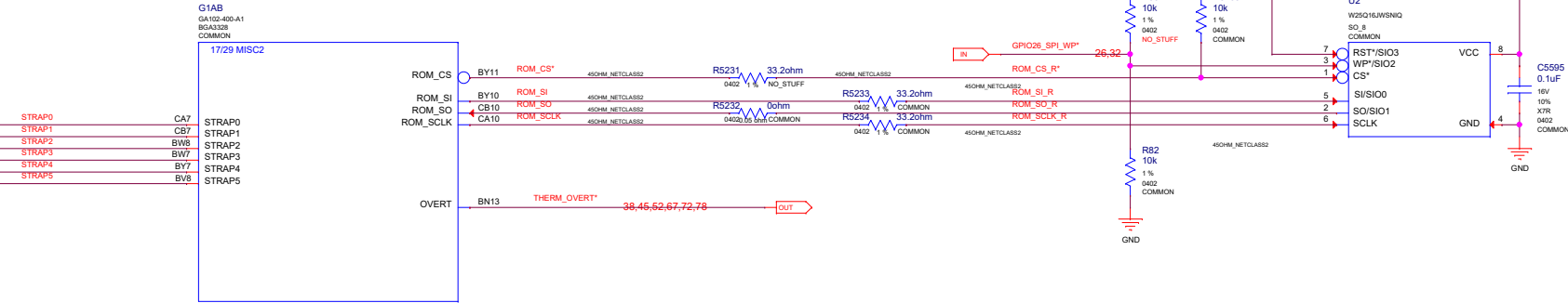
<-OLD

<-LATEST A02 PCB

DEFAULT

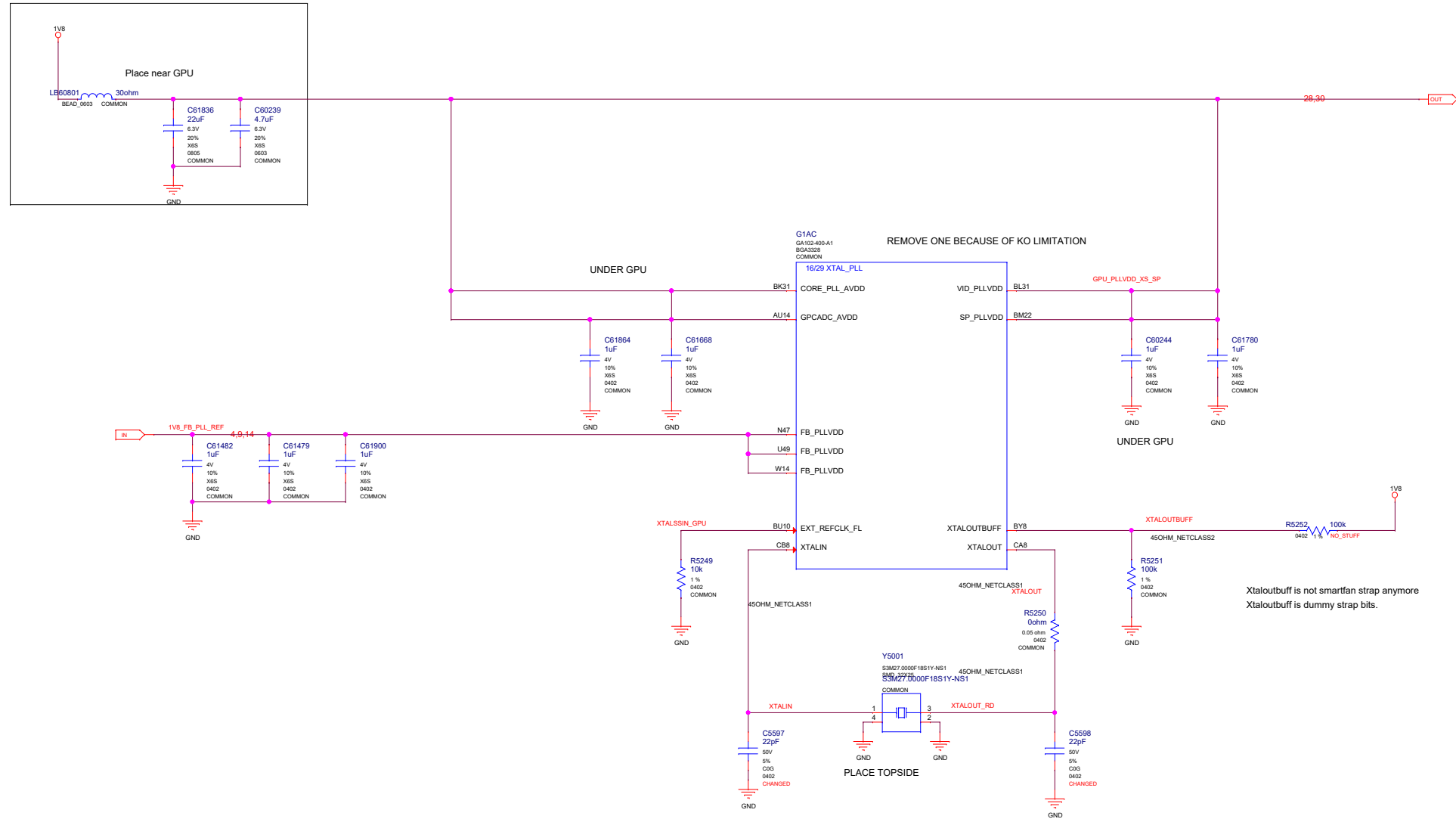
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- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default



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MISC: XTAL. PLL

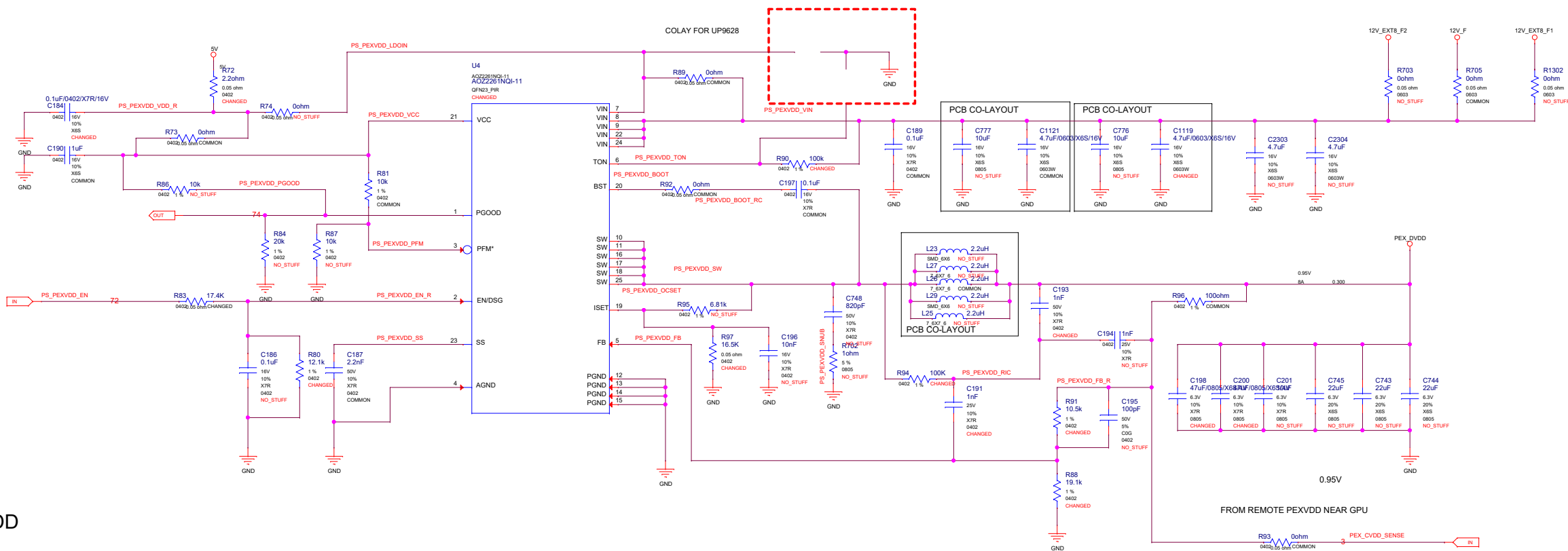


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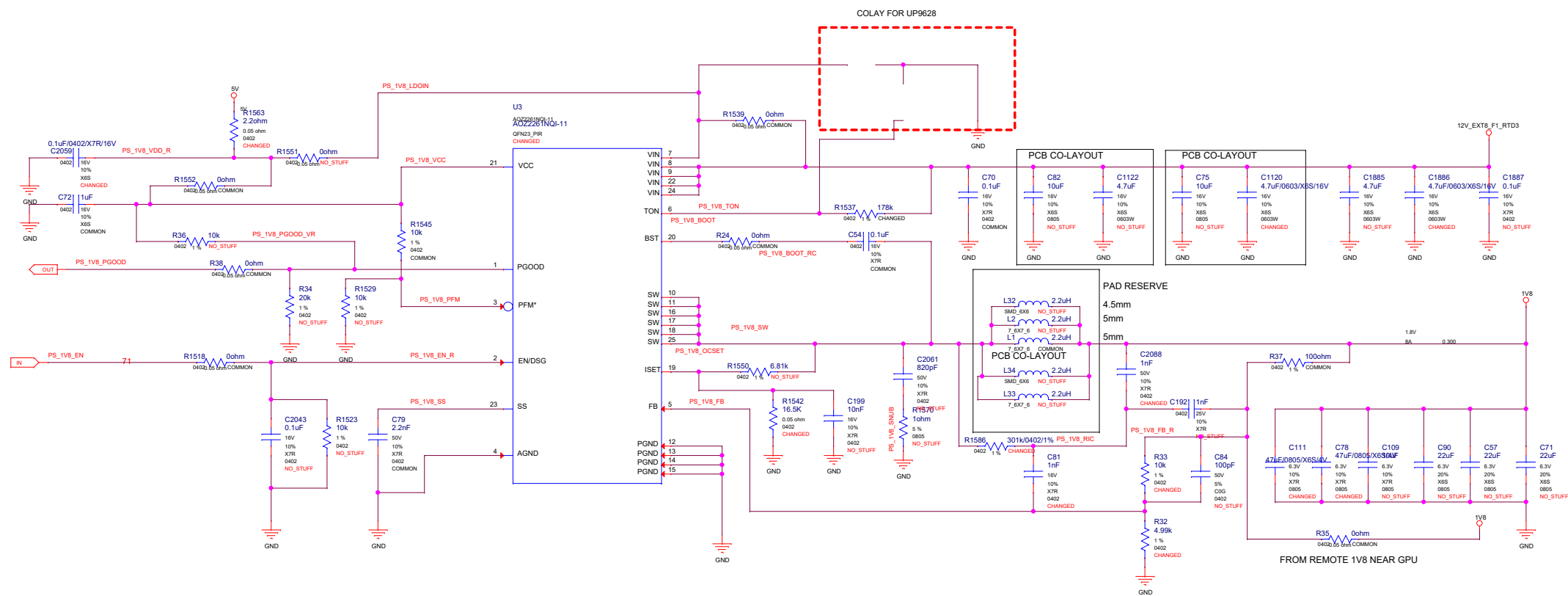


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PS: PEX_DVDD 1V8 Rail



PEX_DVDD



1V8

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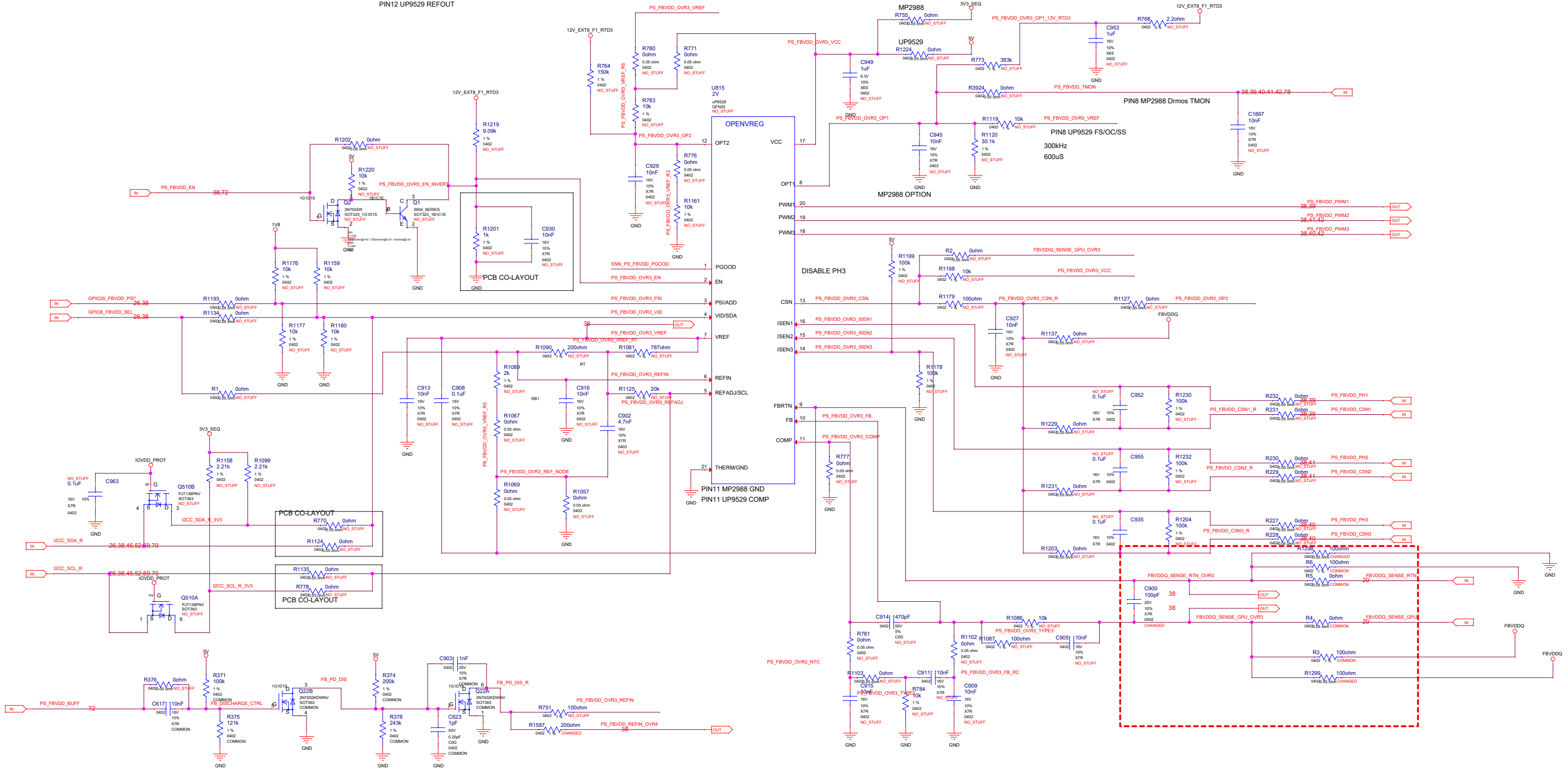
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Custom	GA102HC-E30	A
Date:	Tuesday, July 14, 2020	Sheet 35 of 79

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Date:	Tuesday, July 14, 2020	Sheet 36 of 79															
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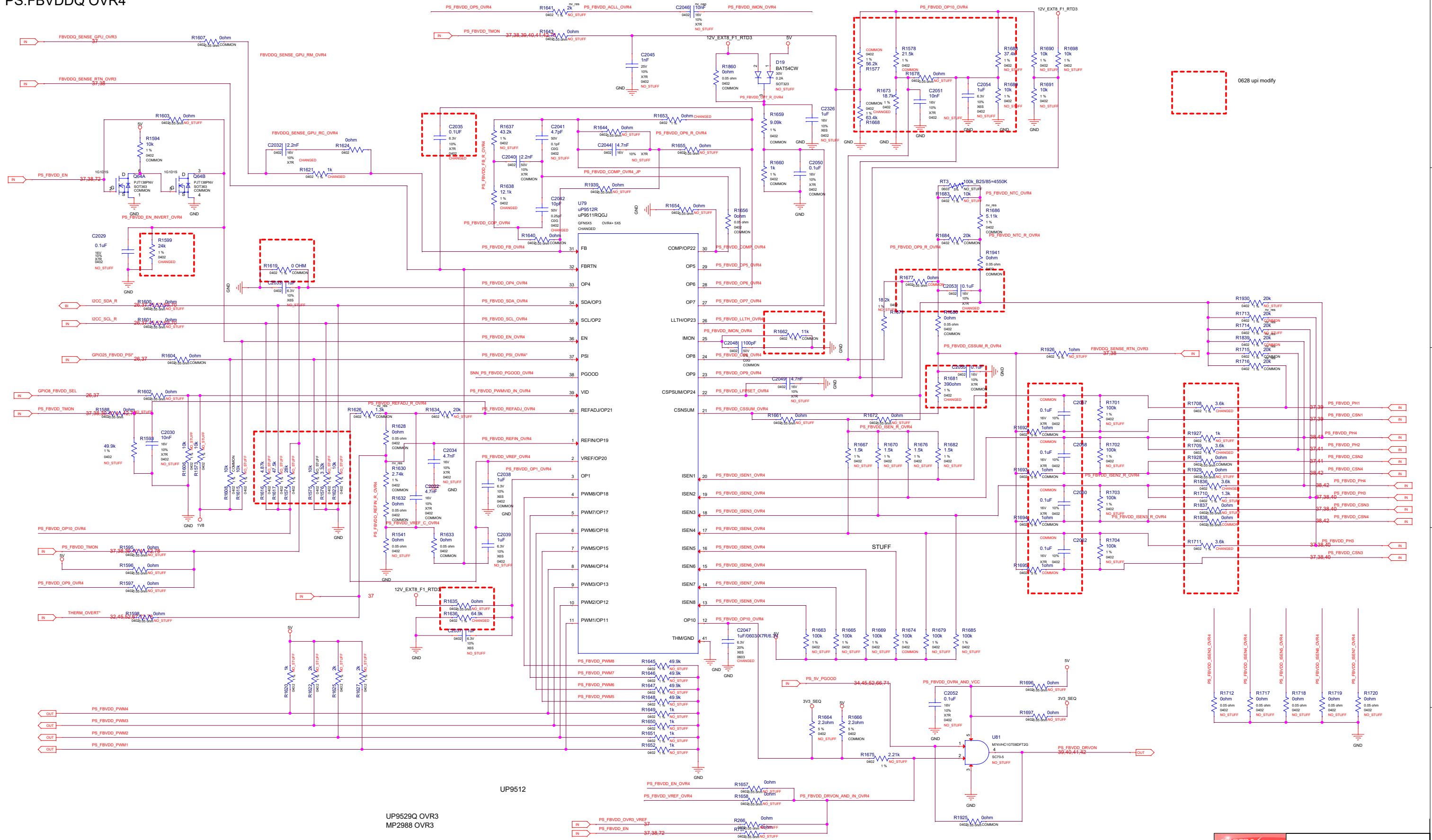
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PIN12 MP2988 VIN SENSE 1/16 DIVIDER
PIN12 UP9529 REFOUT



FOR DT SKU

PS:FBVDDQ OVR4



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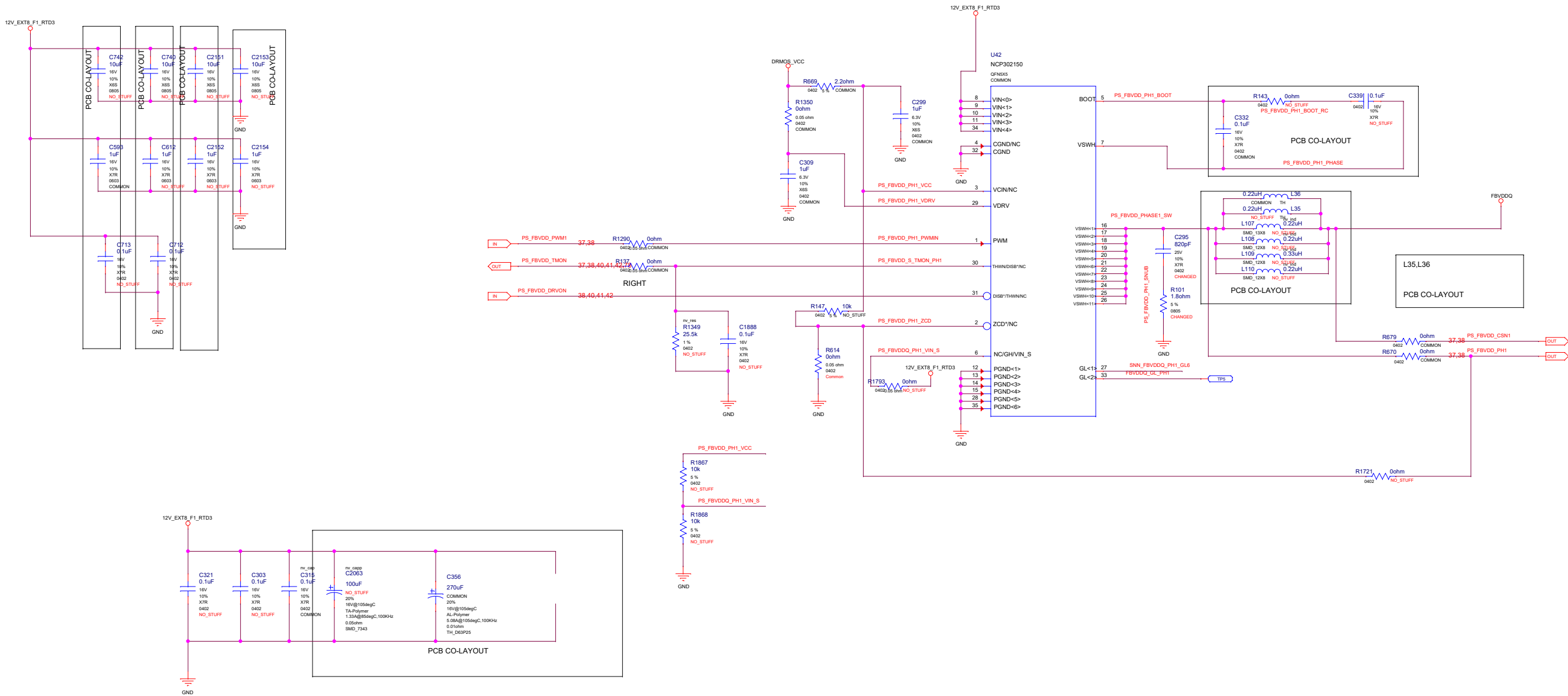
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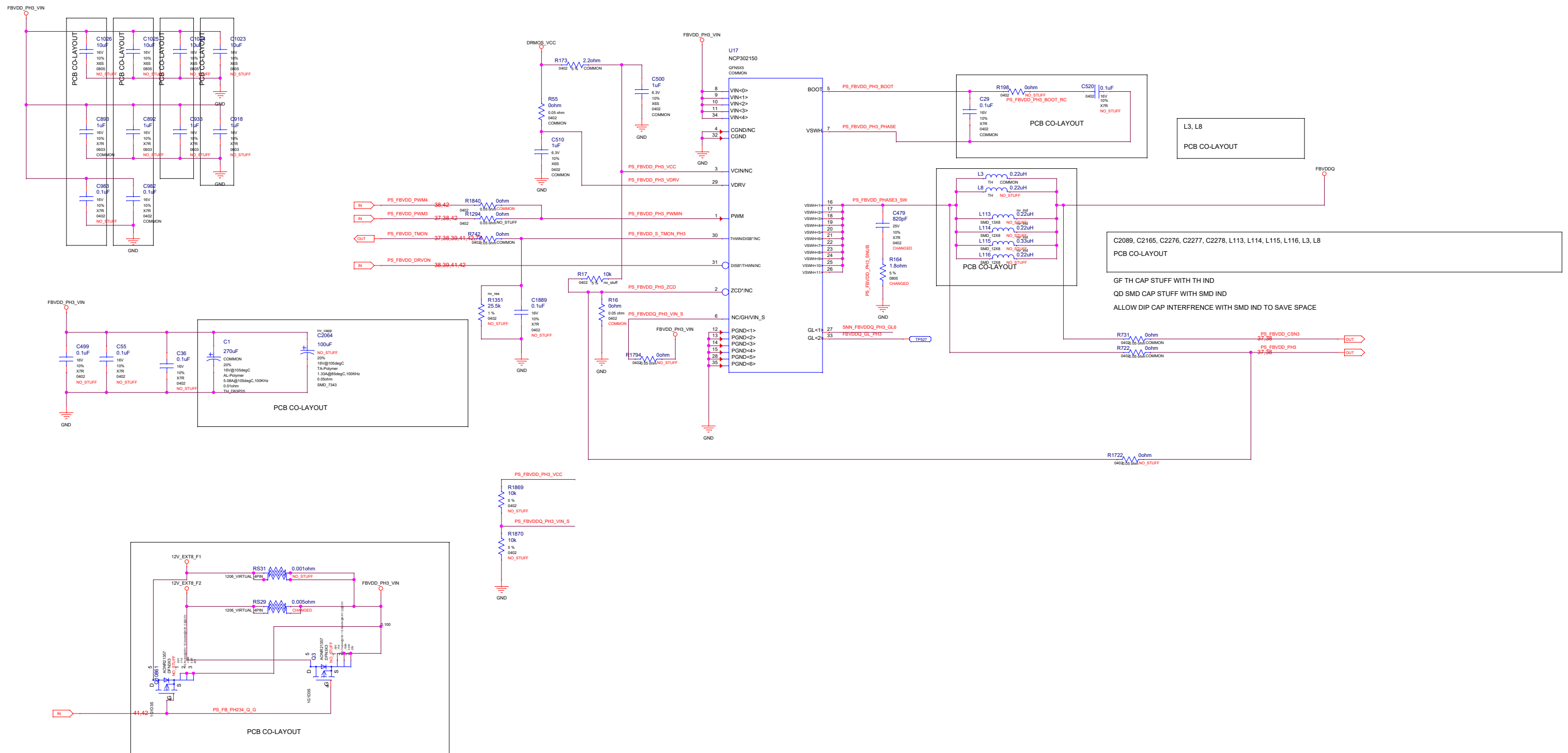
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PS: FBVDD PH1

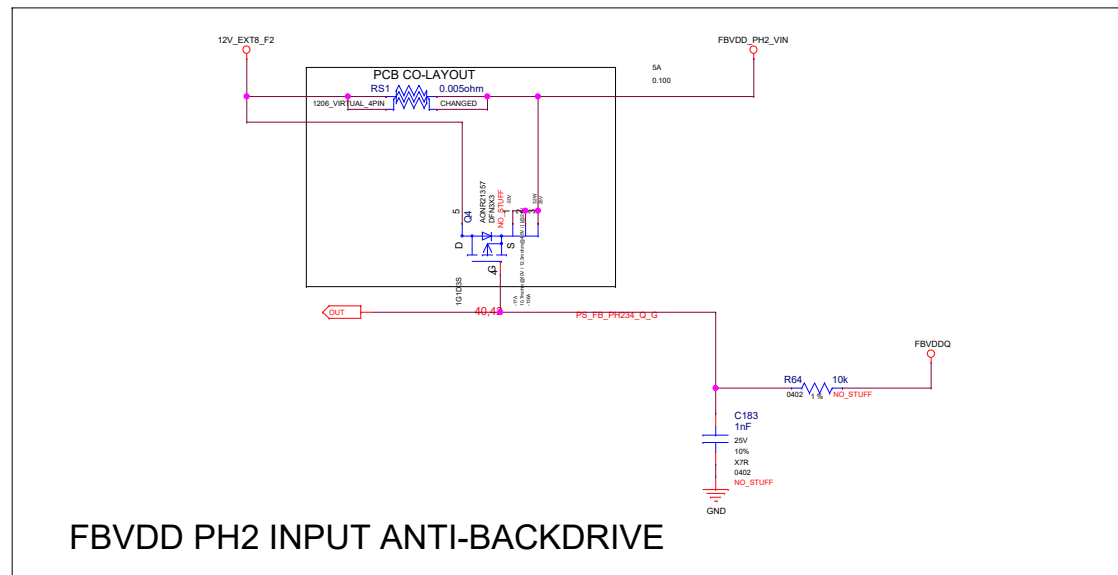
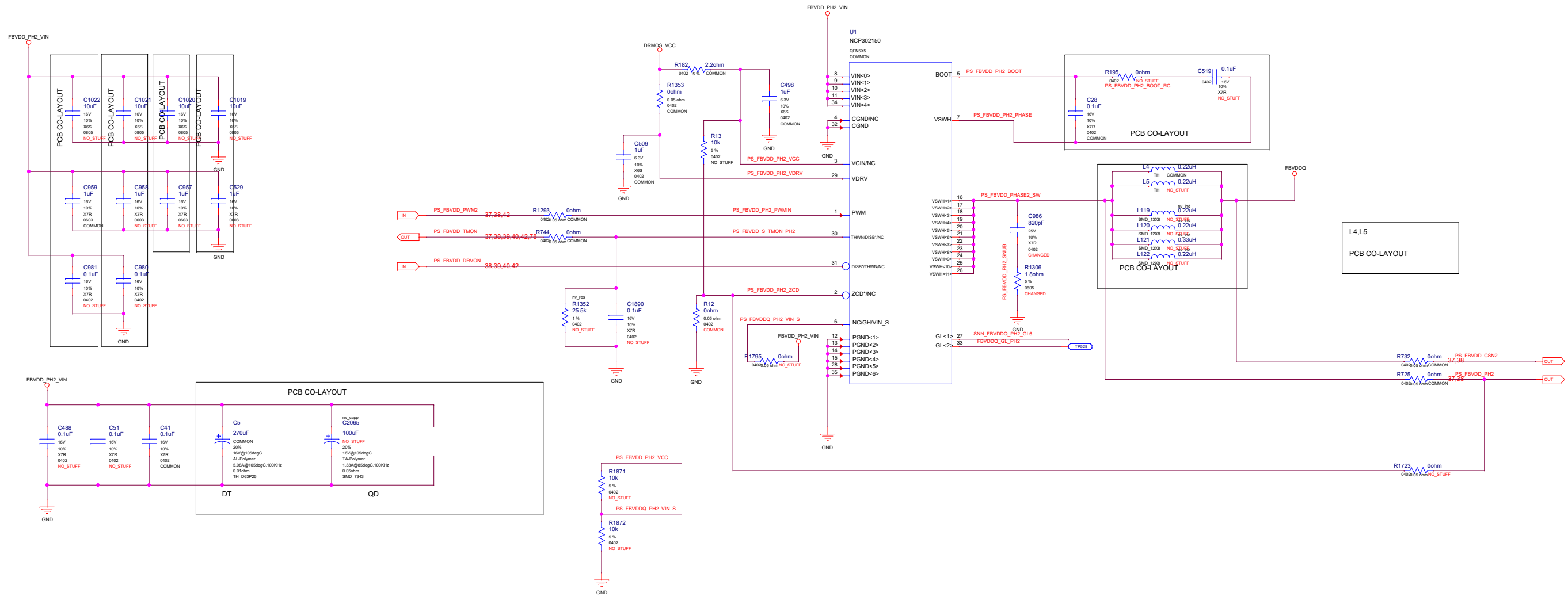


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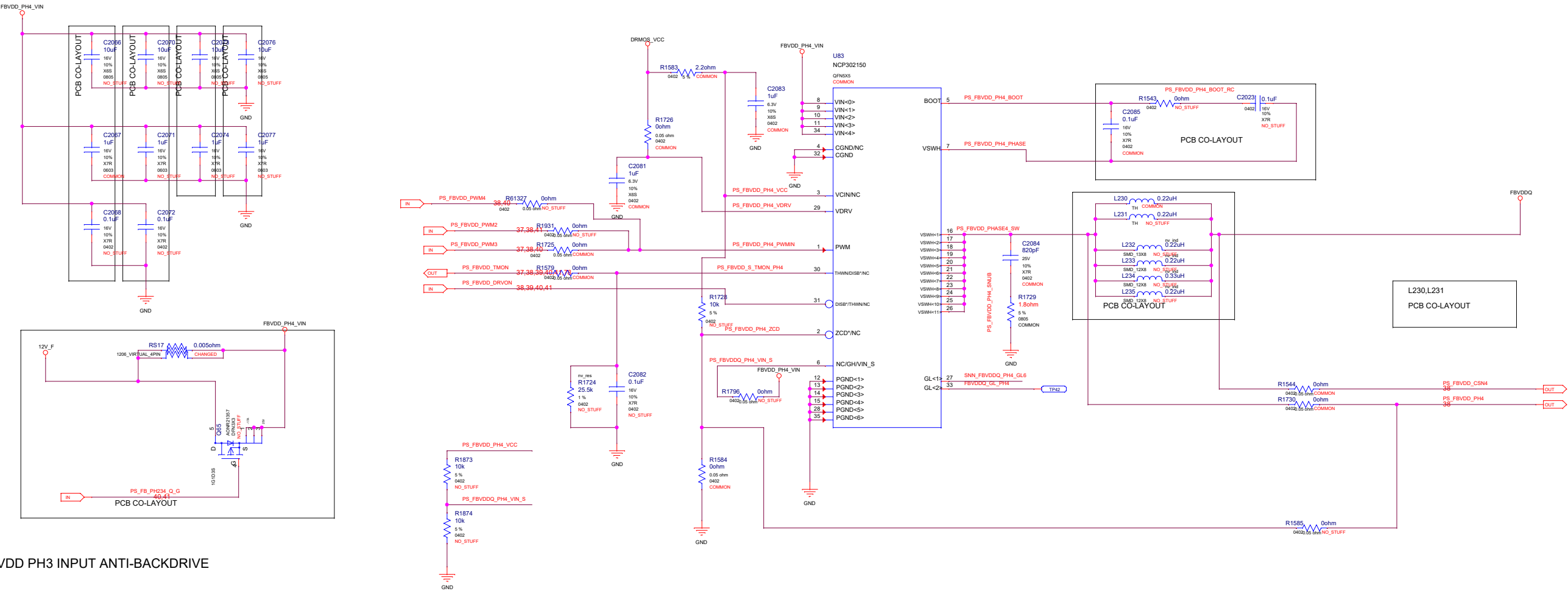


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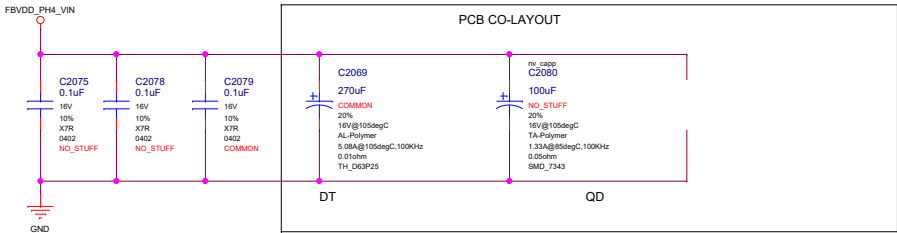
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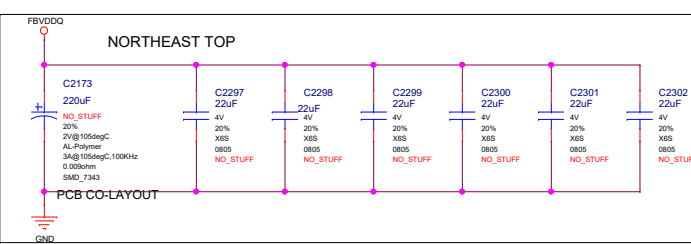
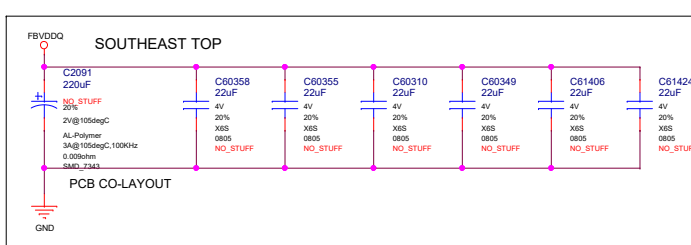
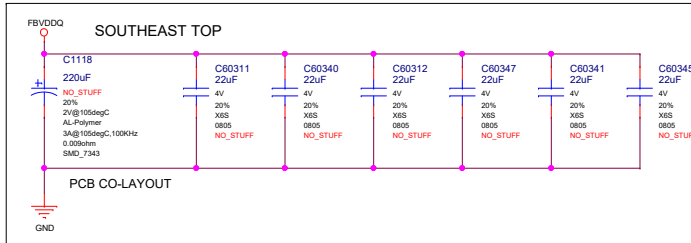
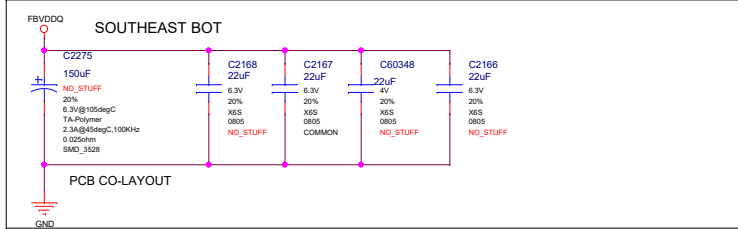
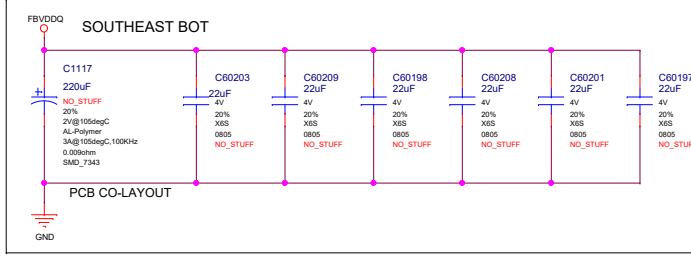
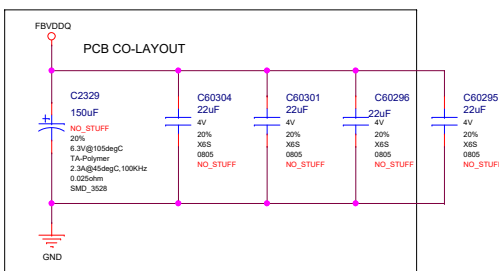
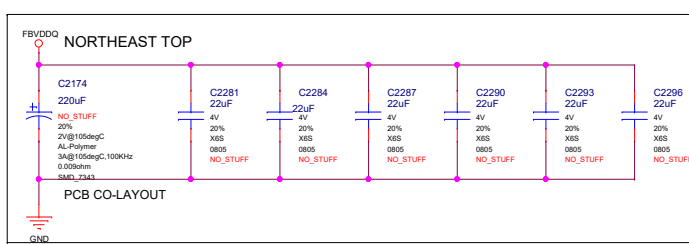
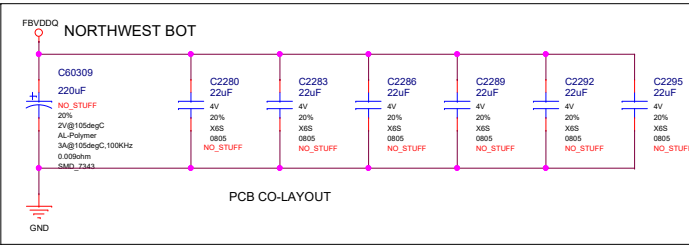
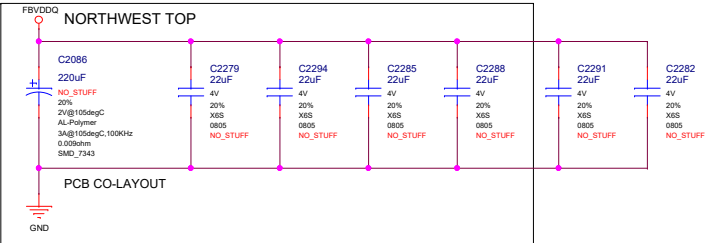
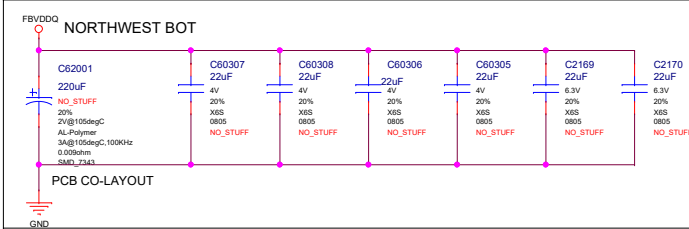
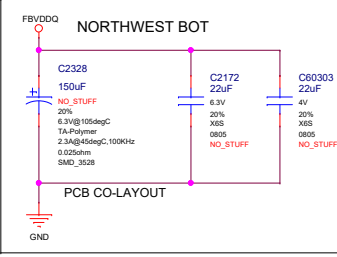
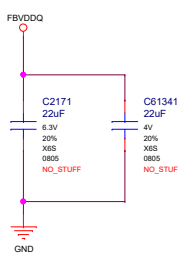
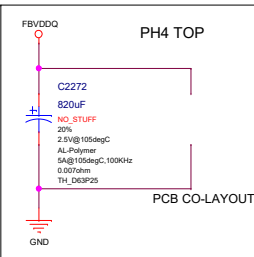
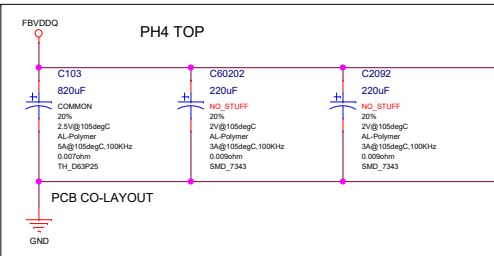
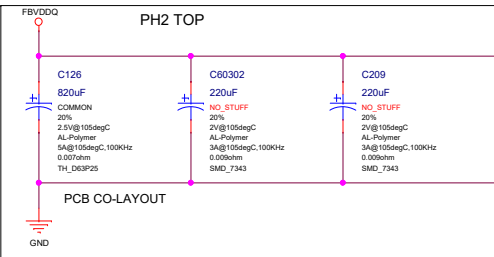
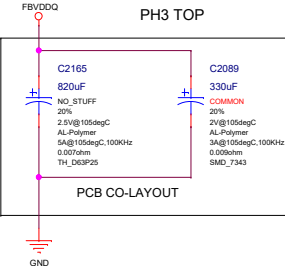
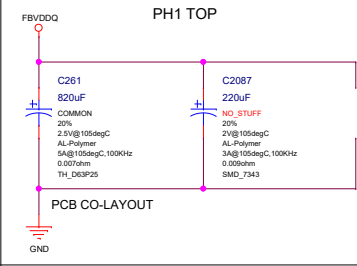


FBVDD PH3 INPUT ANTI-BACKDRIVE



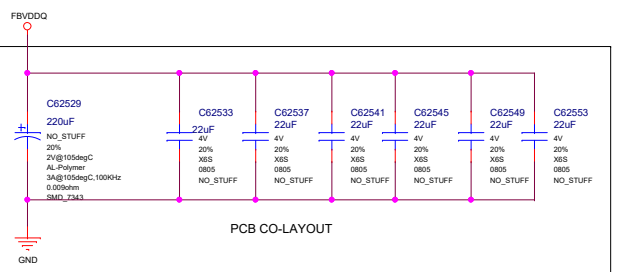
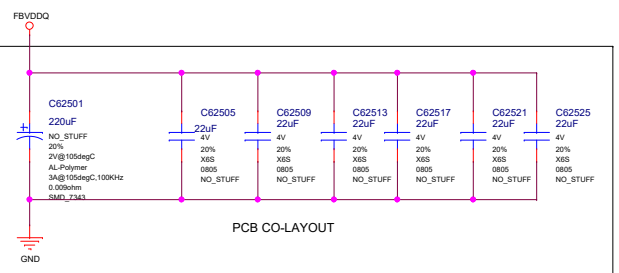
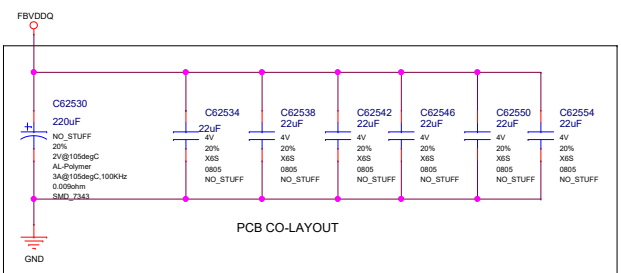
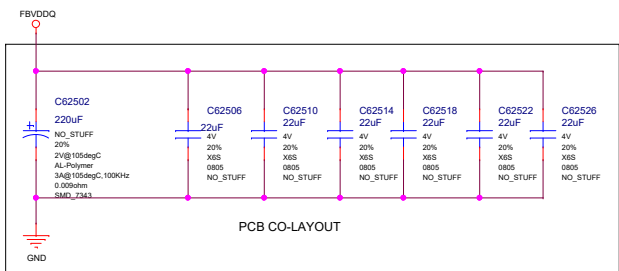
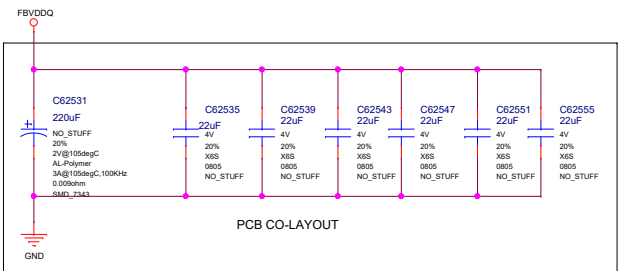
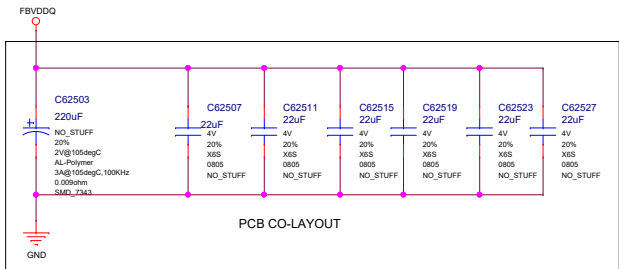
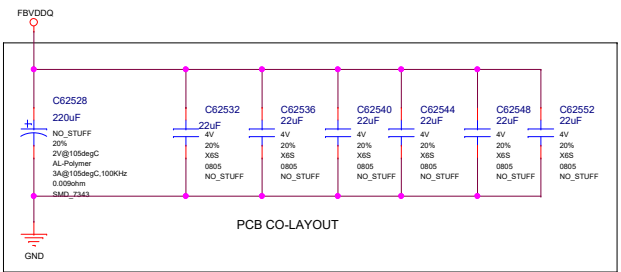
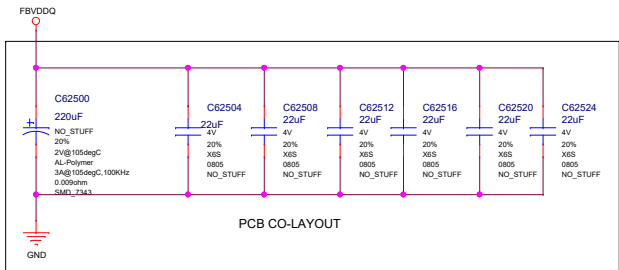
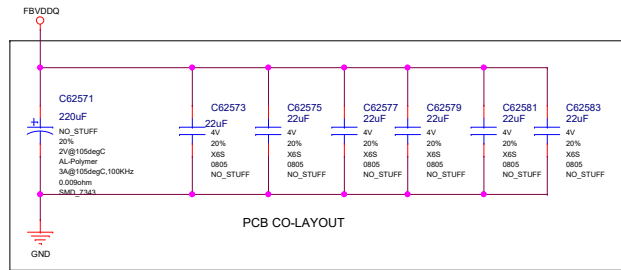
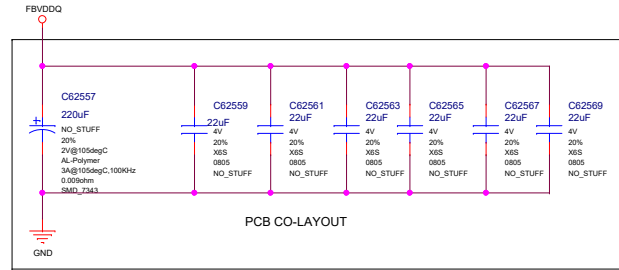
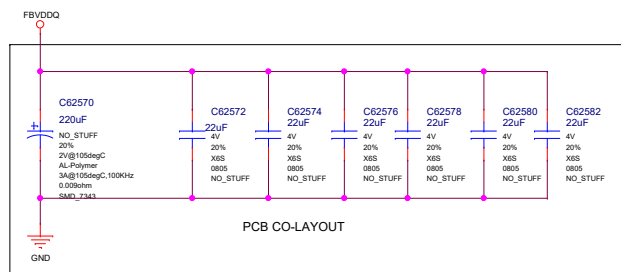
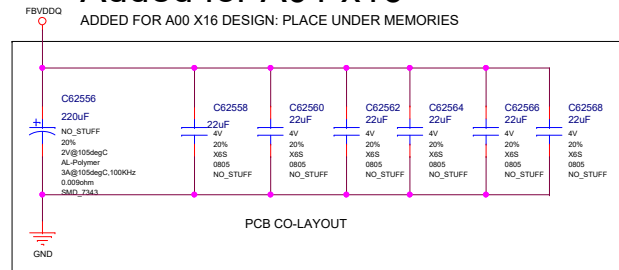
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3x 820uF TH FBVDD OUTPUT BULK CAPS

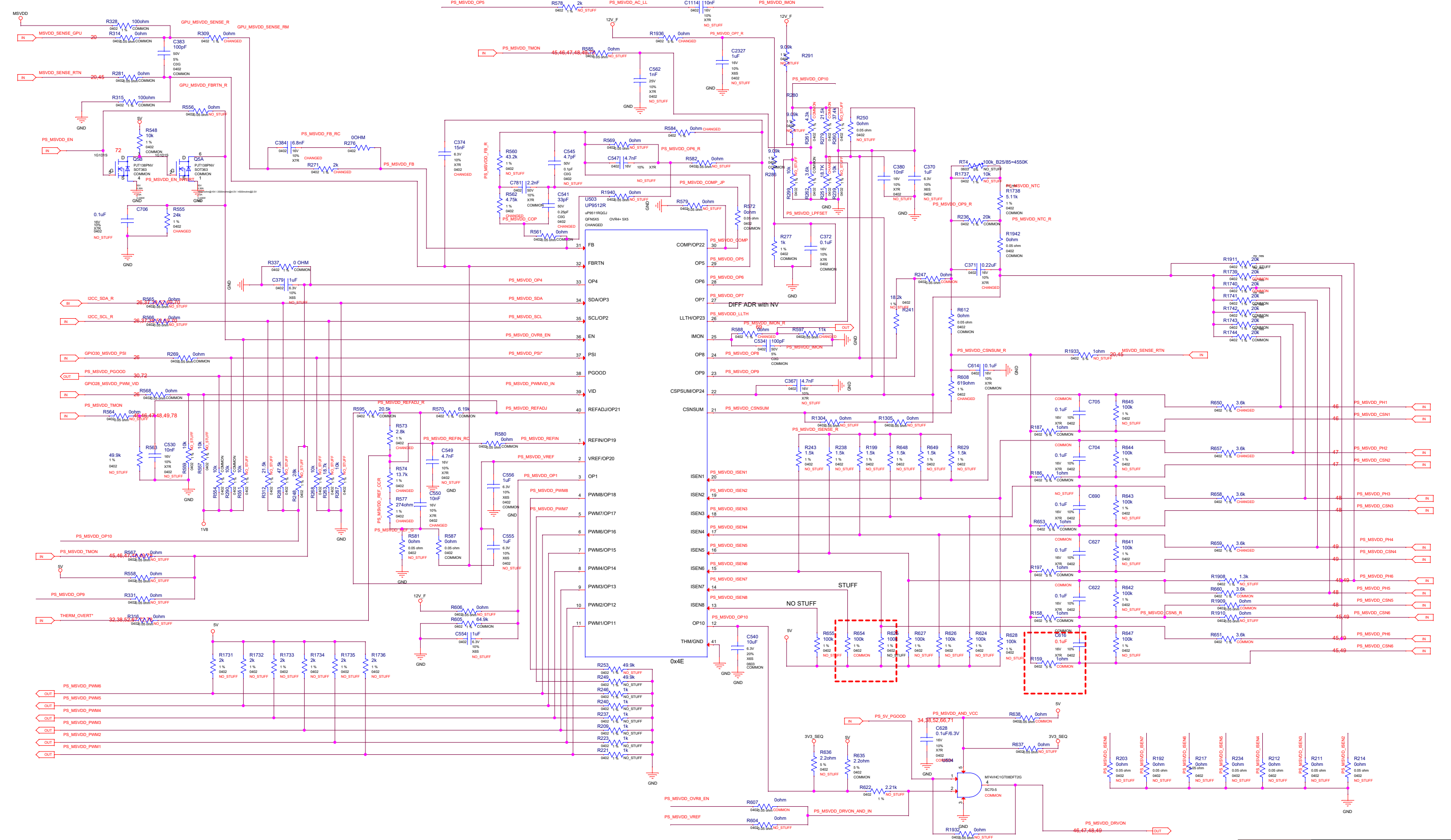


Added for A01 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES




PS: MSVDD



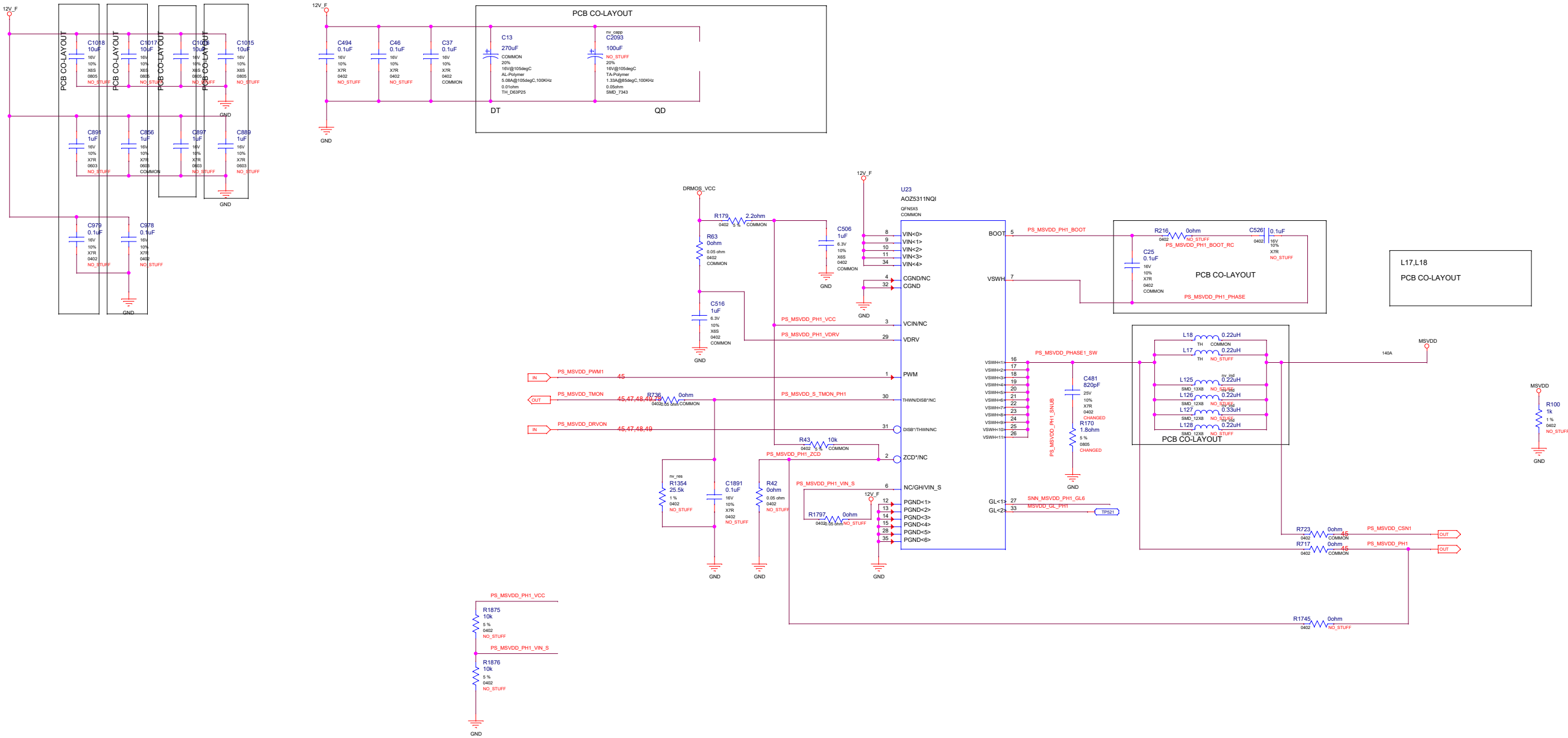
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PS: MSVDD Phase 1

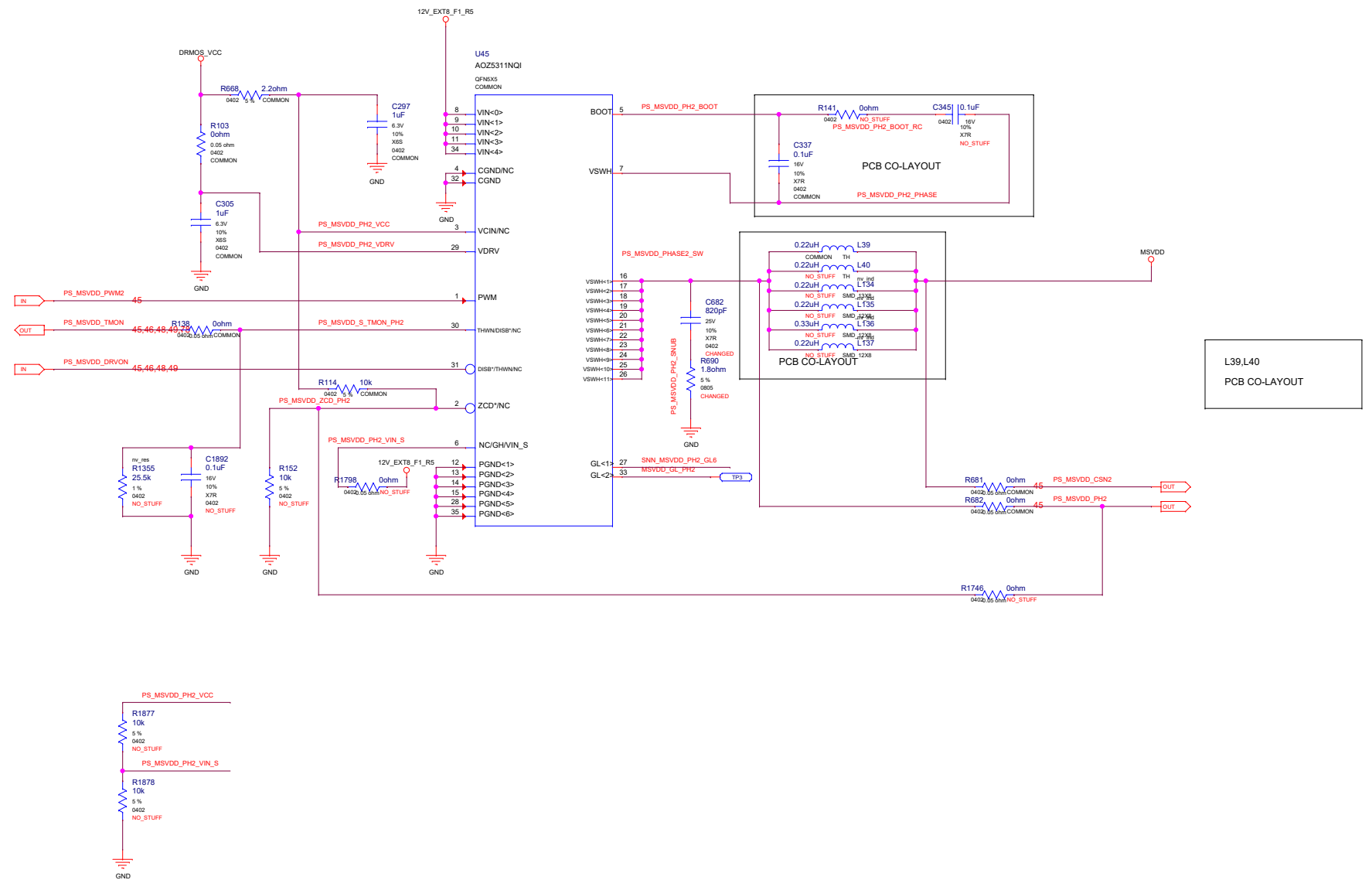
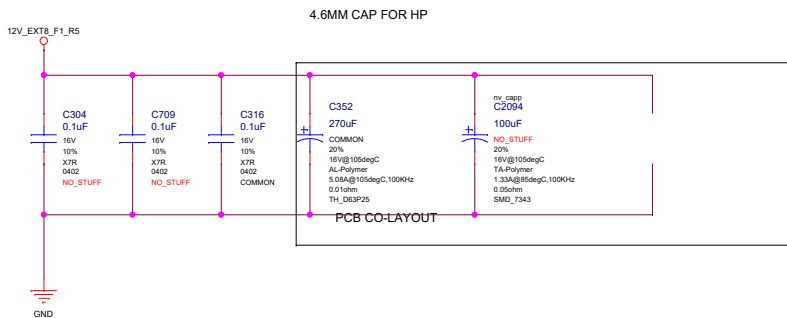
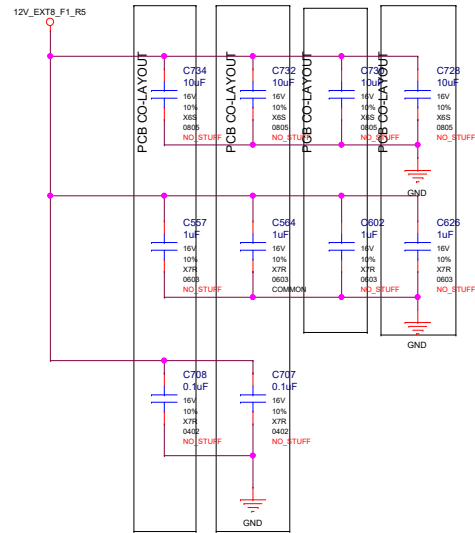


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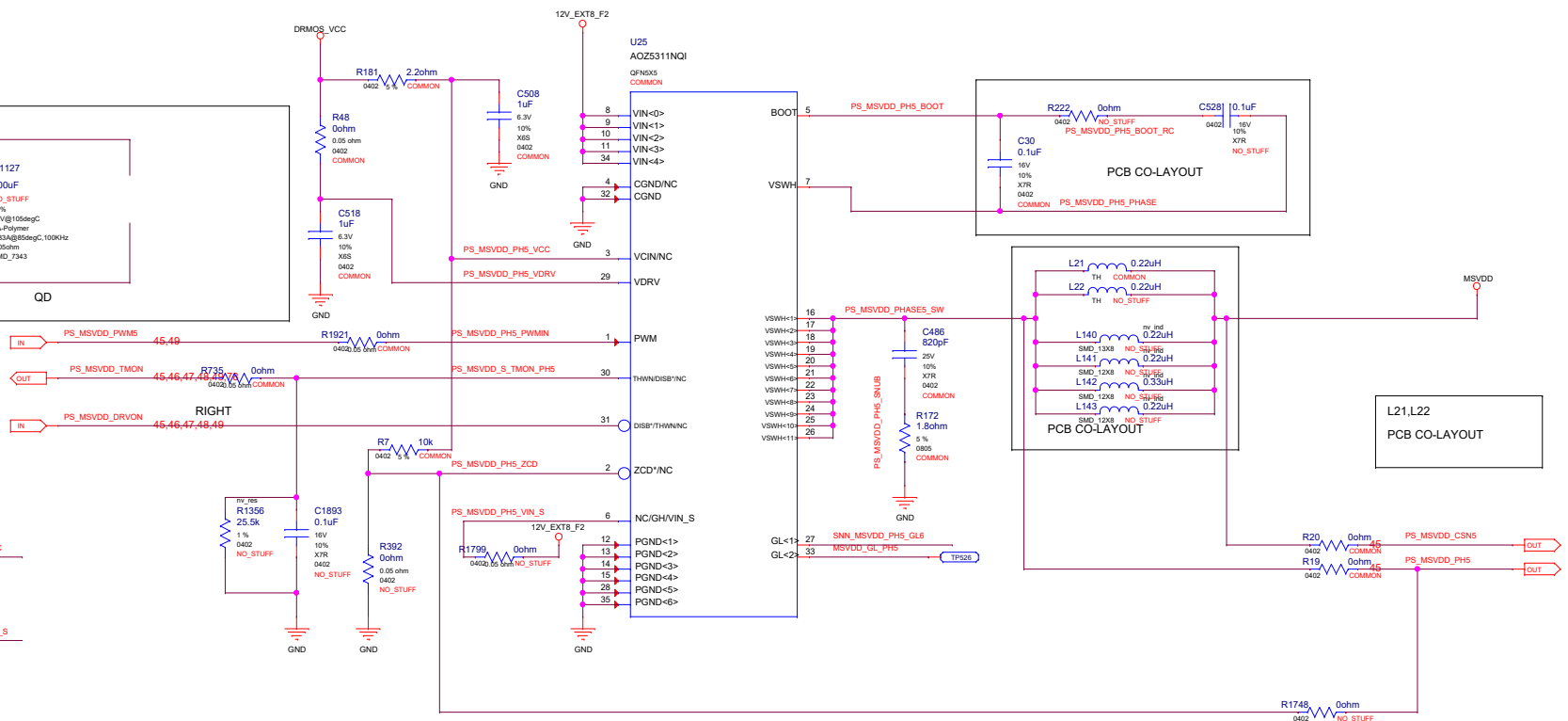
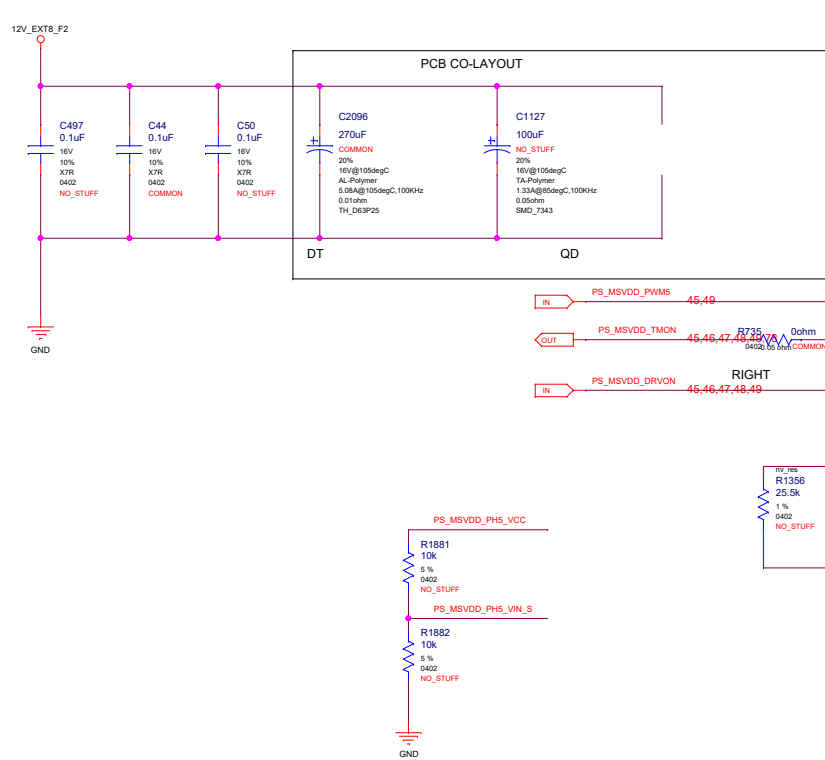
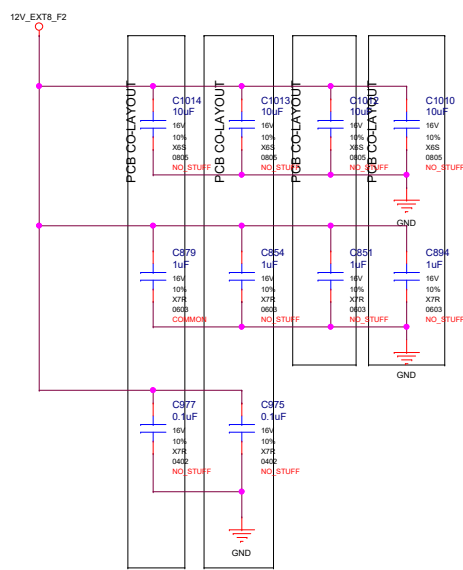
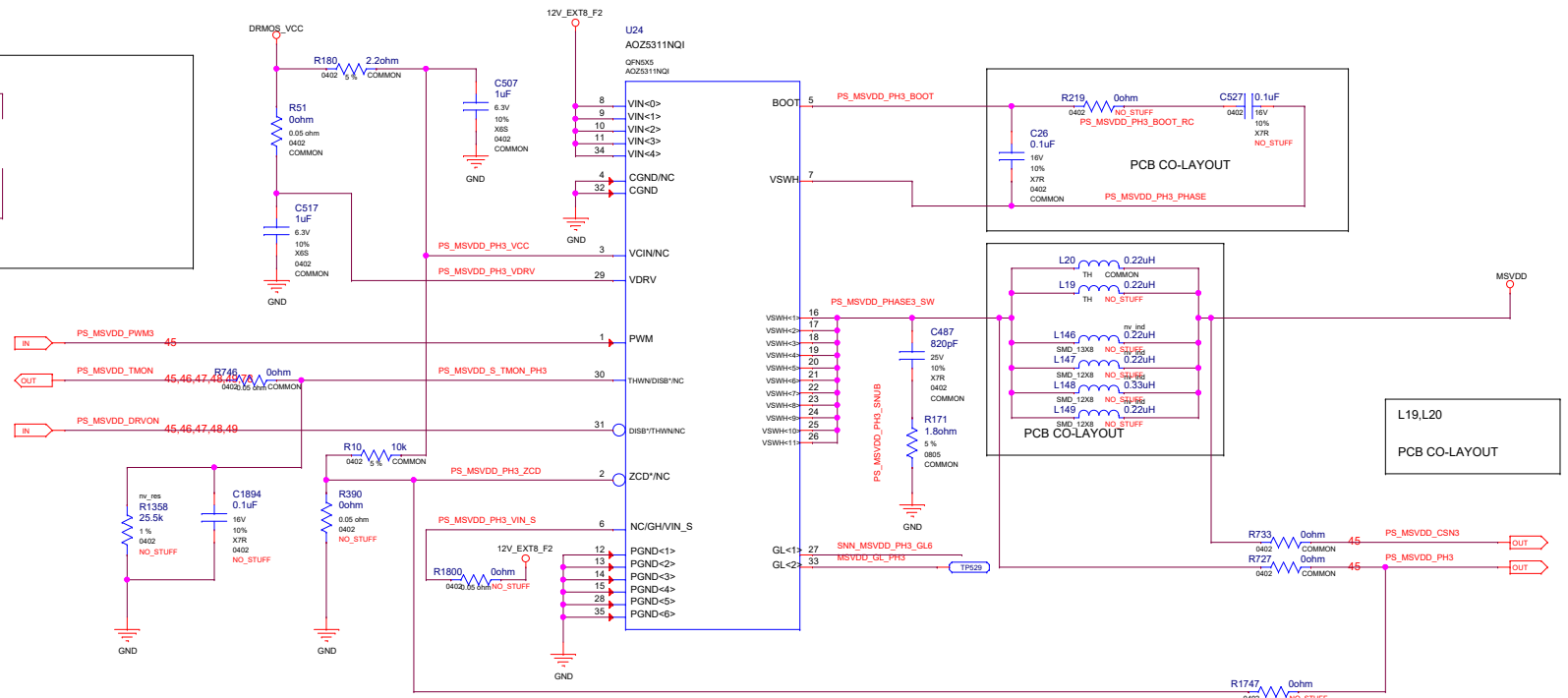
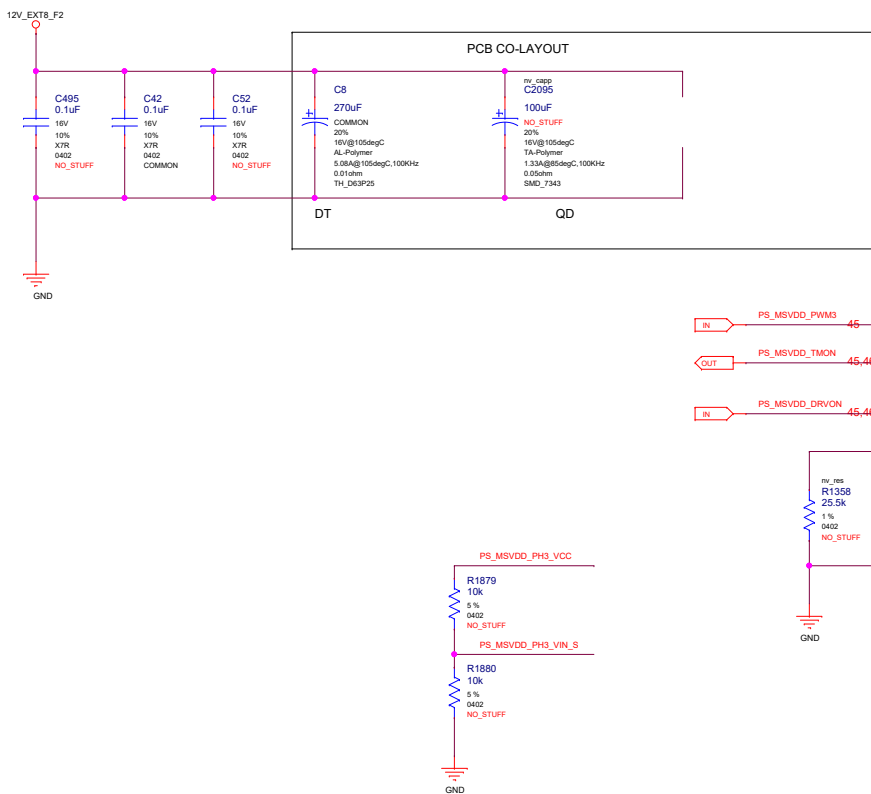
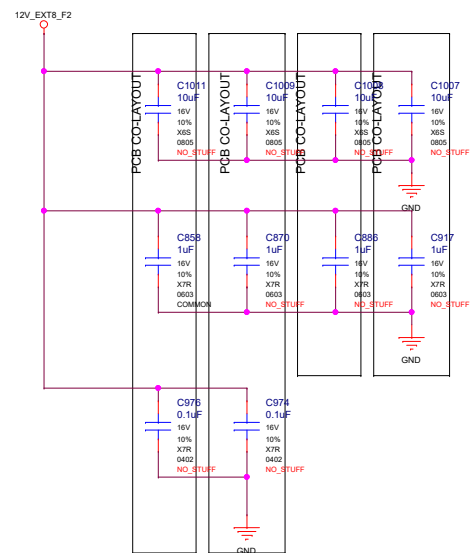
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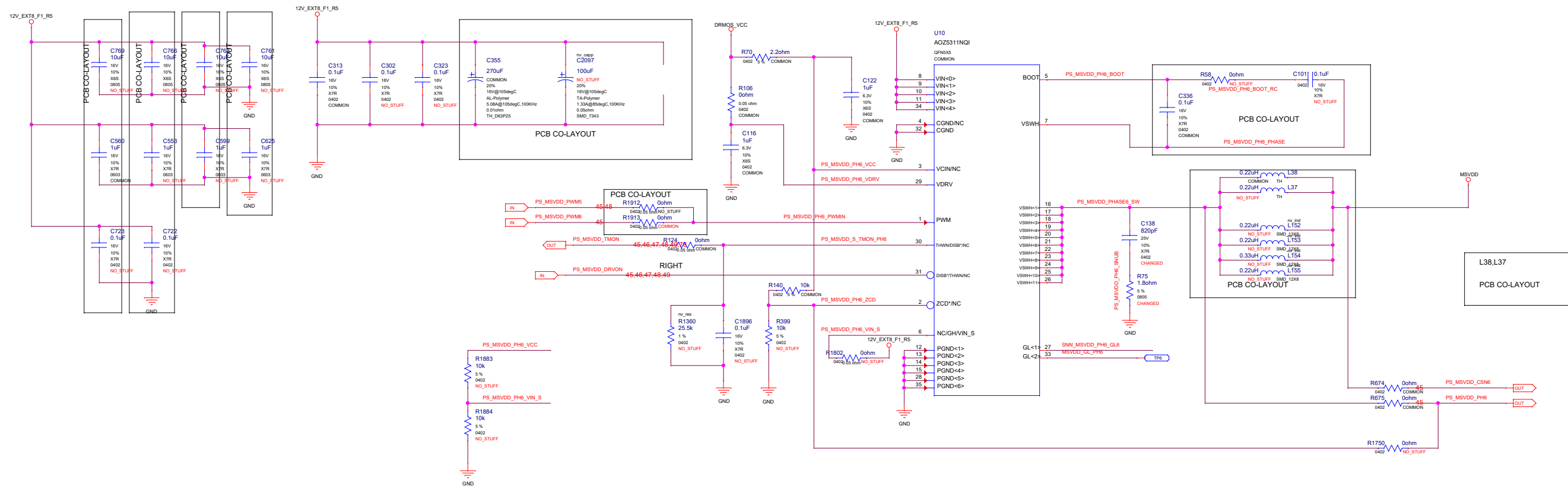
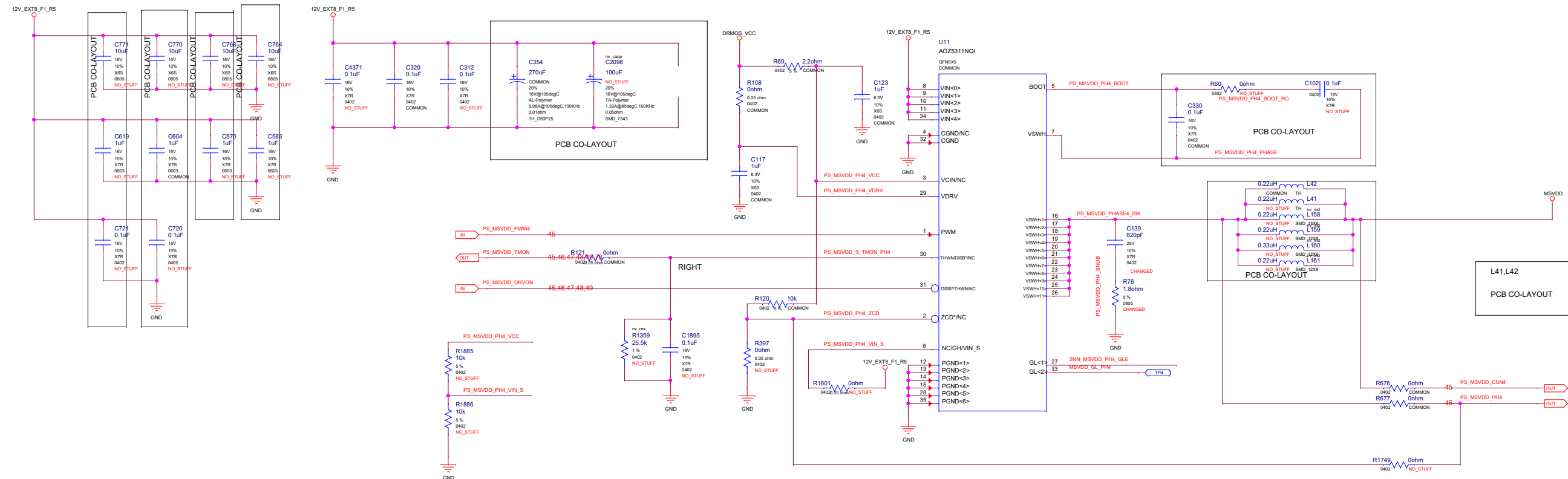
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PS:MSVDD Phase 3, 5



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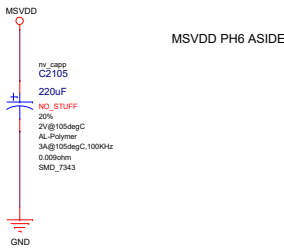
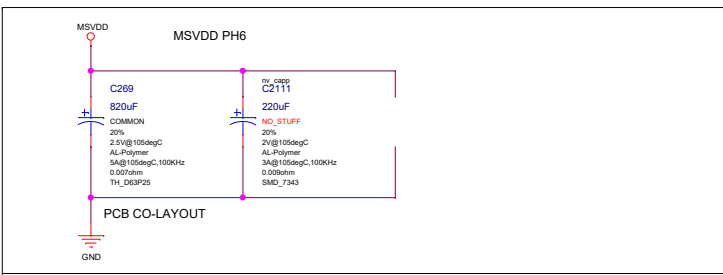
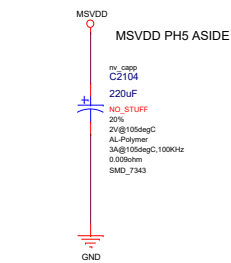
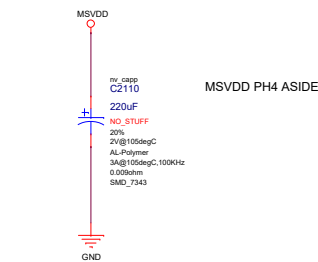
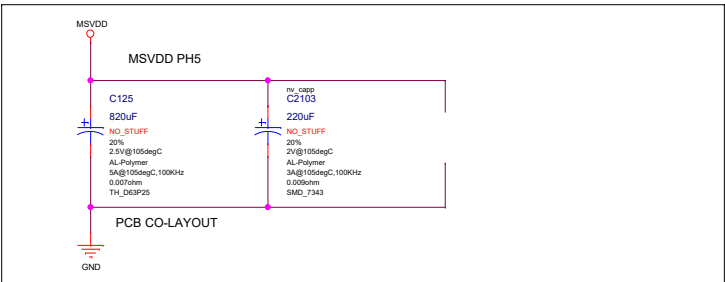
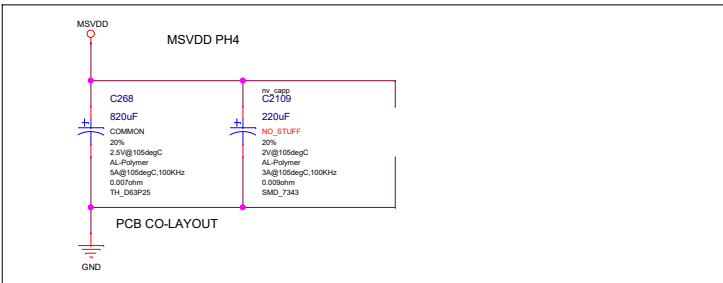
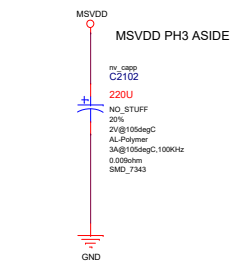
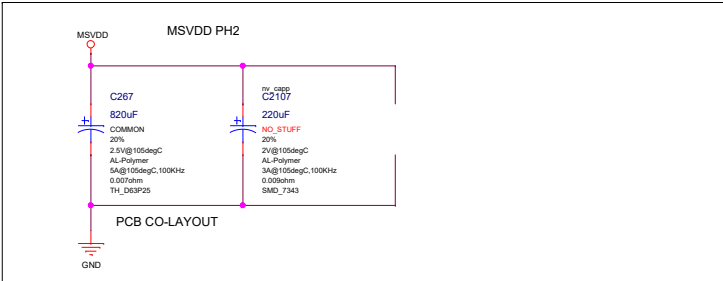
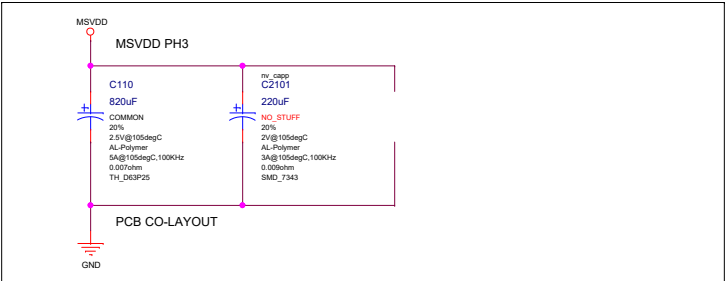
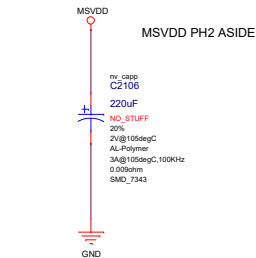
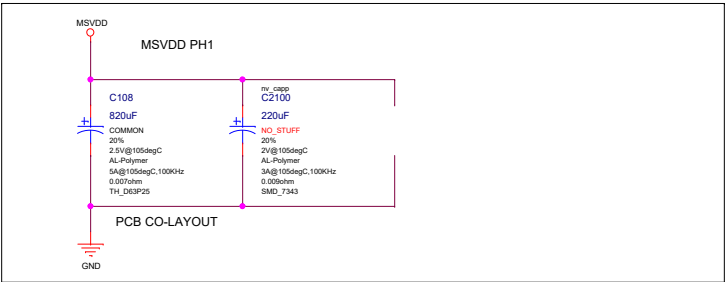
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PS:MSVDD OUTPUT CAP (TOP)



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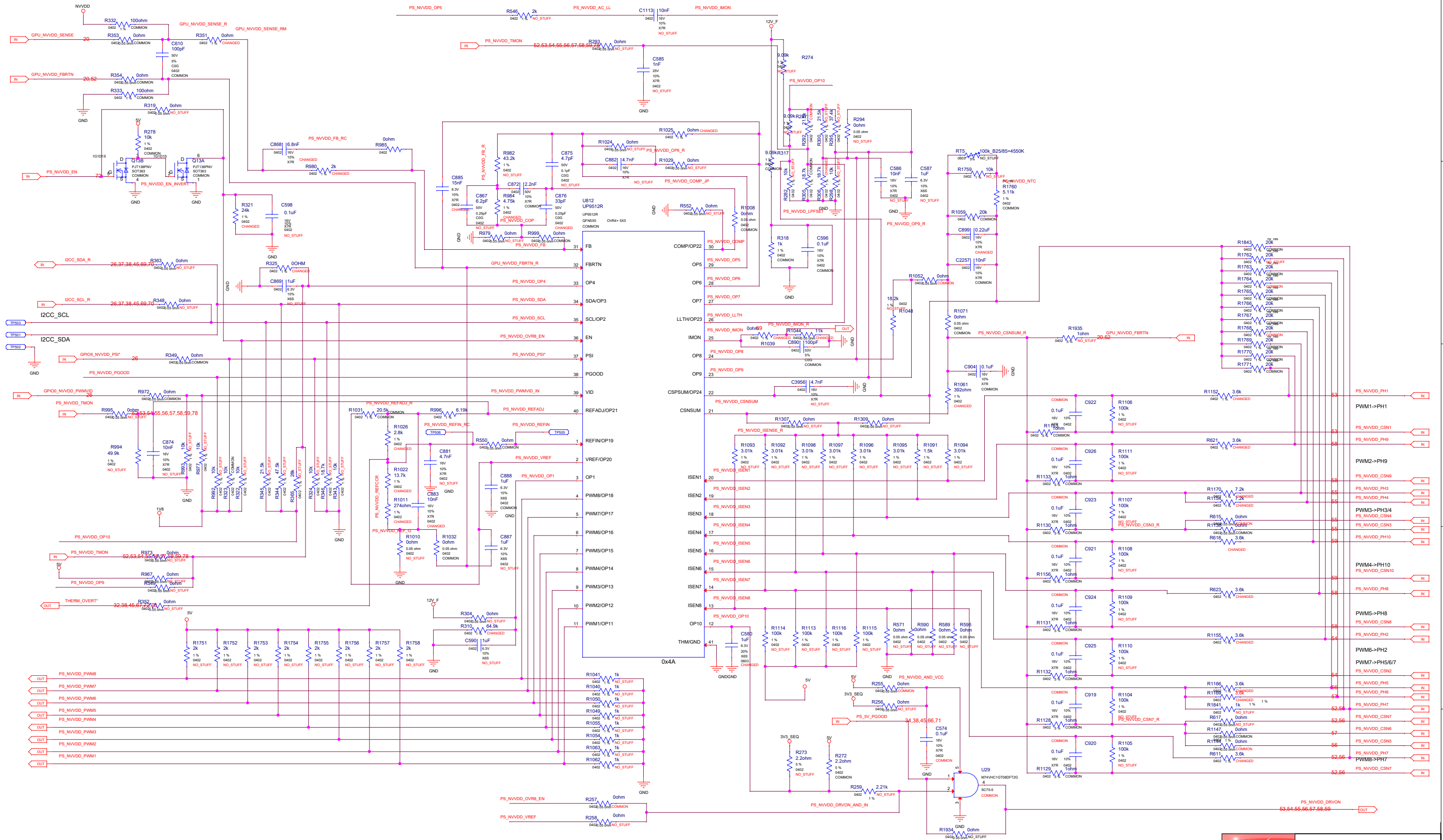
RD Center - MB Department

Colorful Co.,Ltd

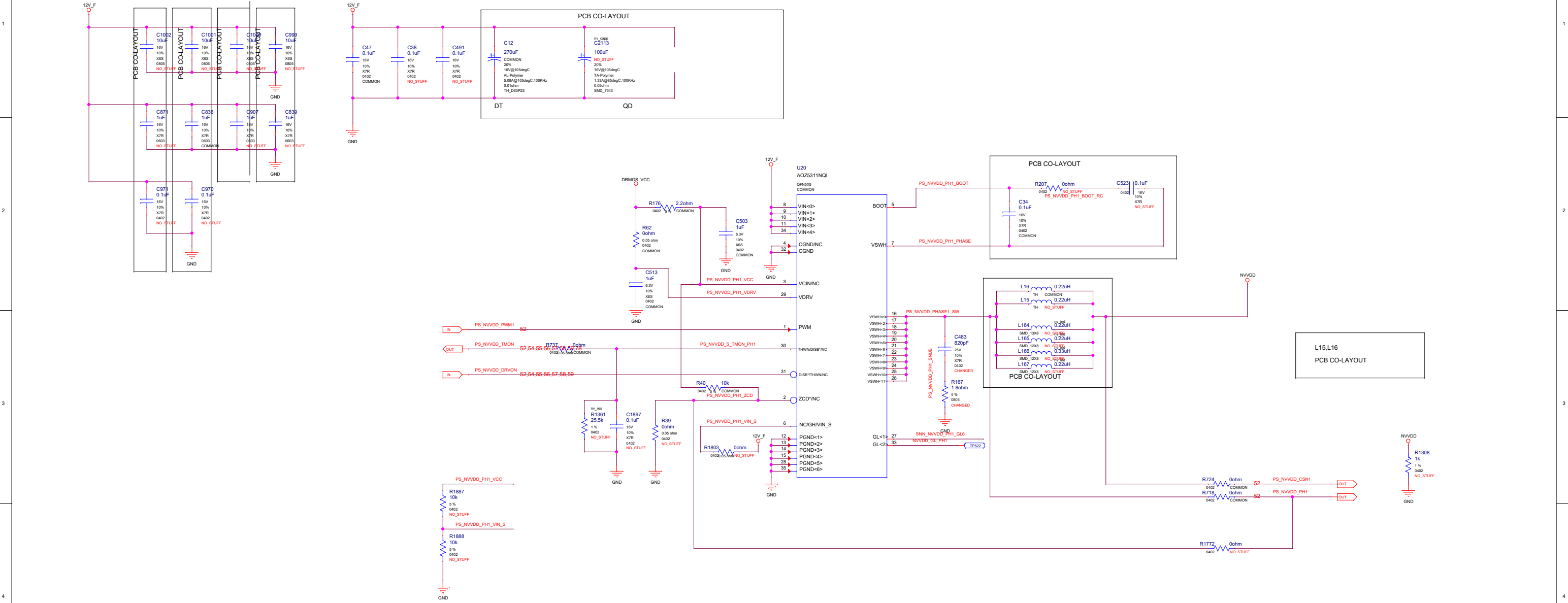
深圳市七彩虹科技发展有限公司

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Date:	Tuesday, July 14, 2020	Sheet 51 of 79

PS: NVVDD Controller_OVR8

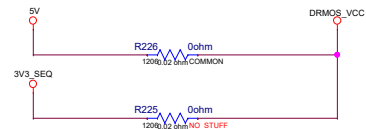


PS: NVVDD Phase 1

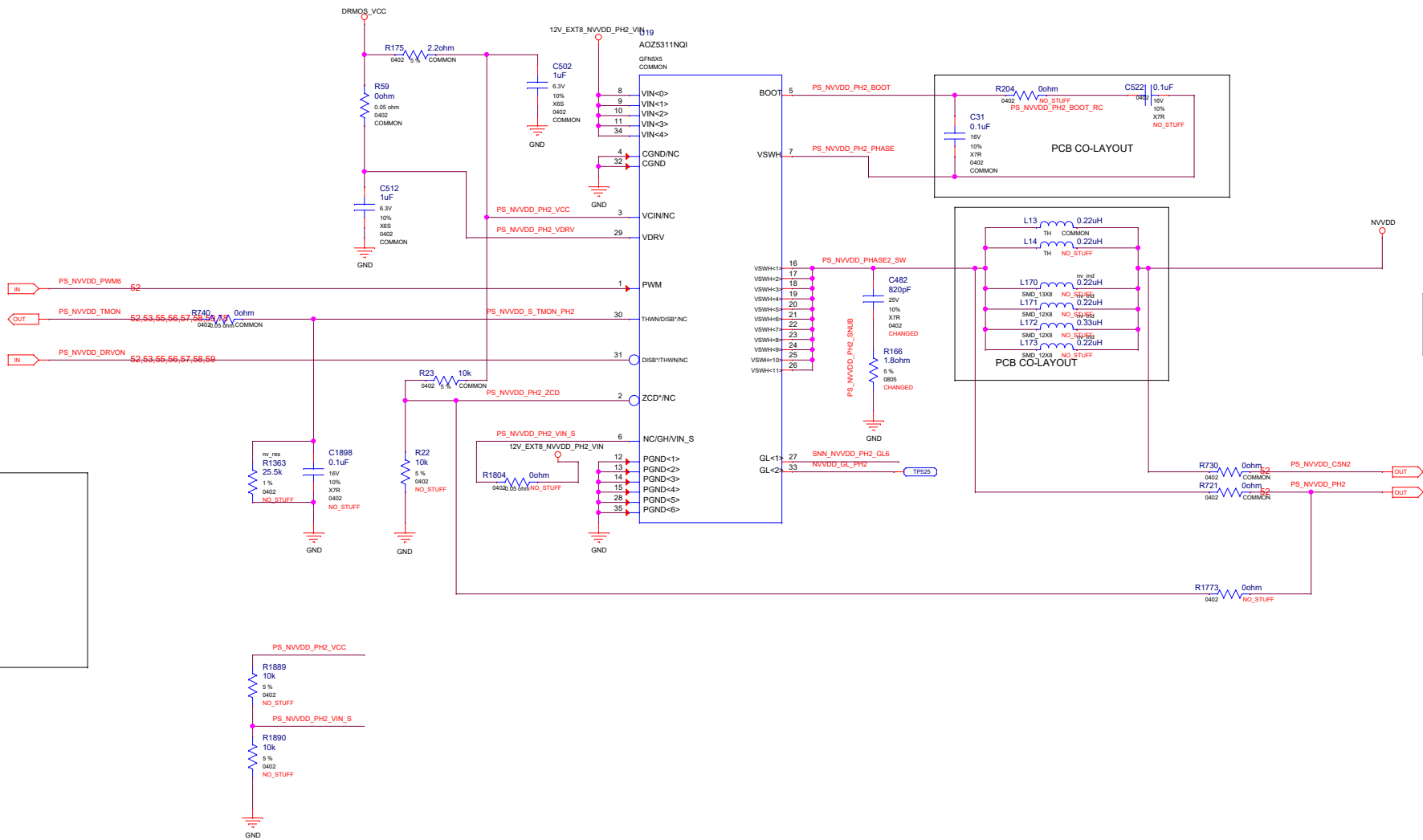
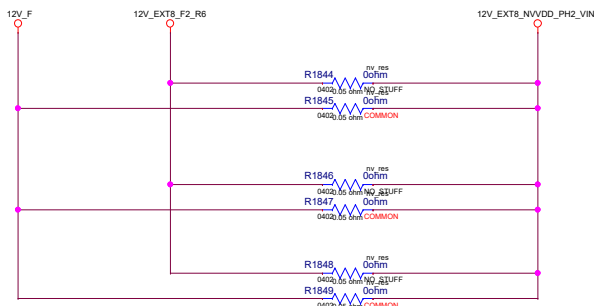
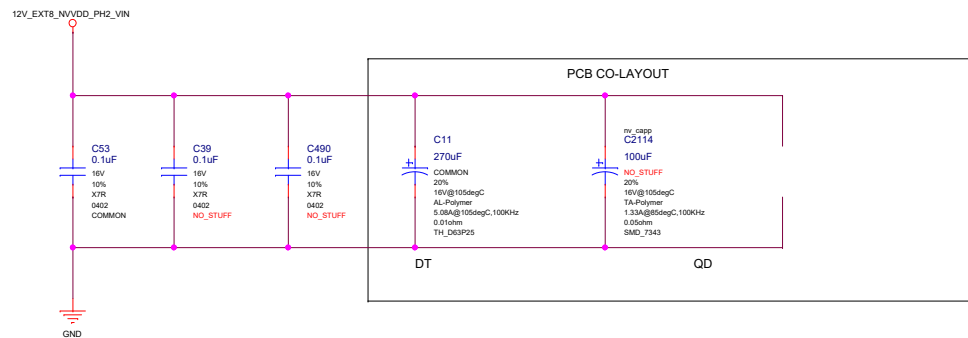
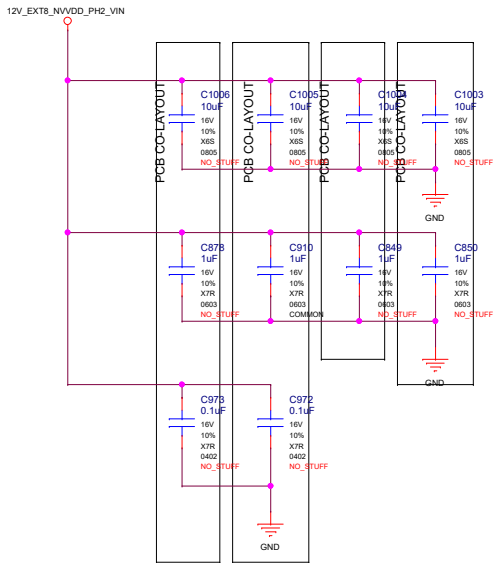


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PS: NVVDD Phase 2



MPS DRMos WITH 3V3 SUPPLY

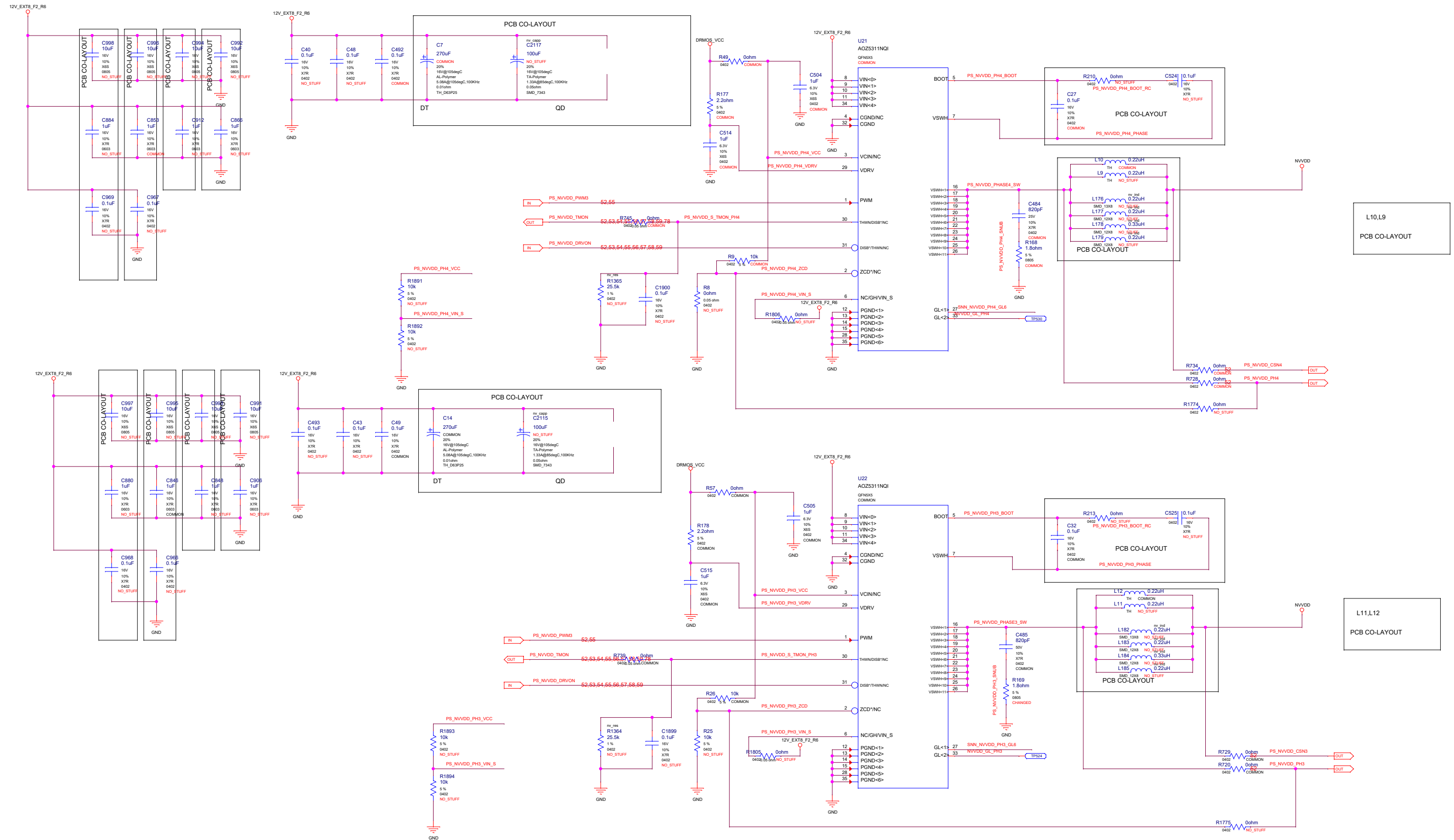


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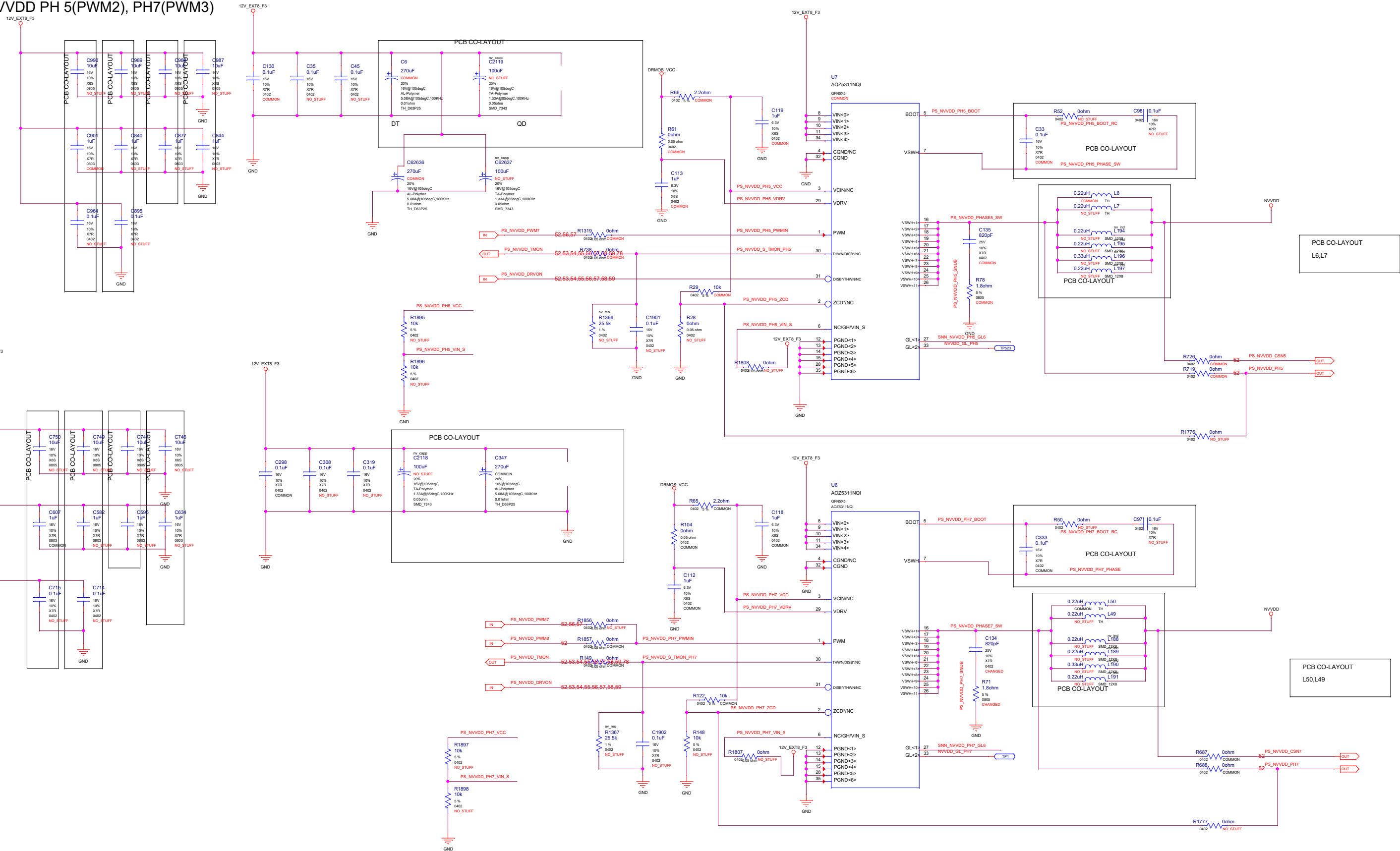
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PS: NVVDD
PH2(PWM6)

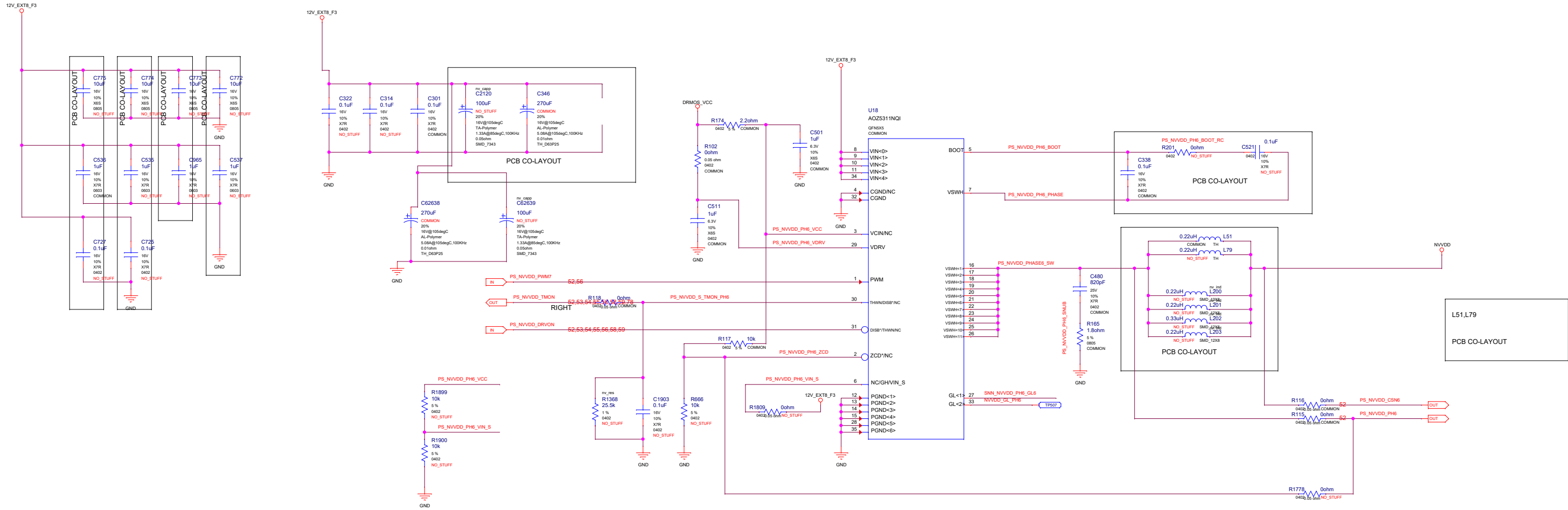
PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)



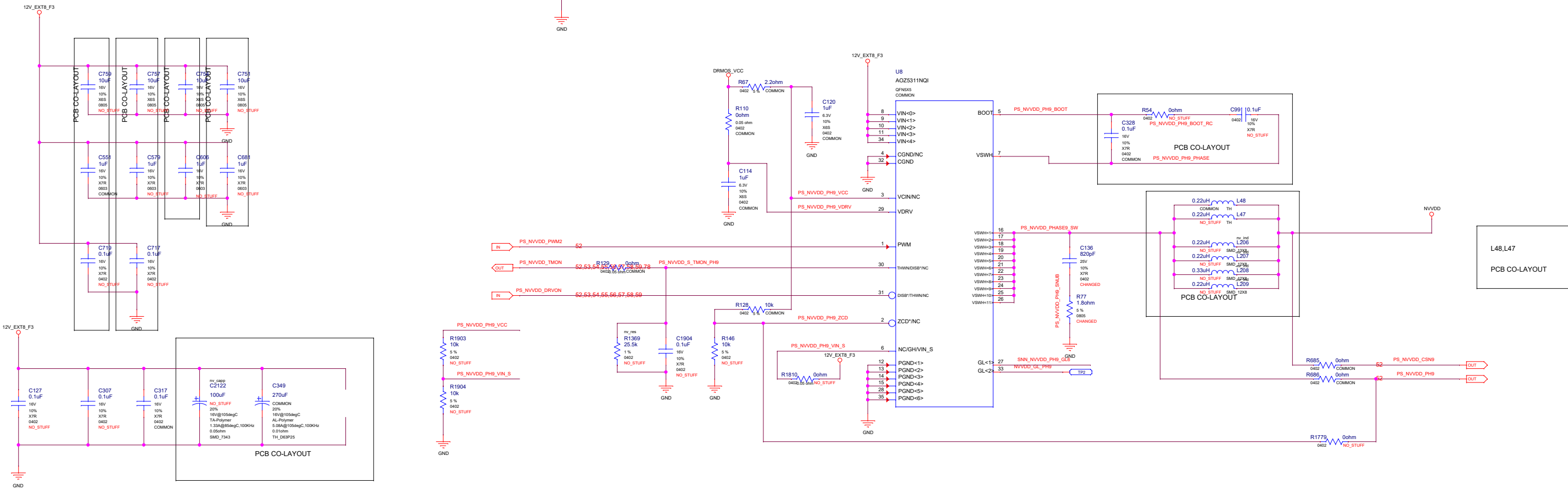
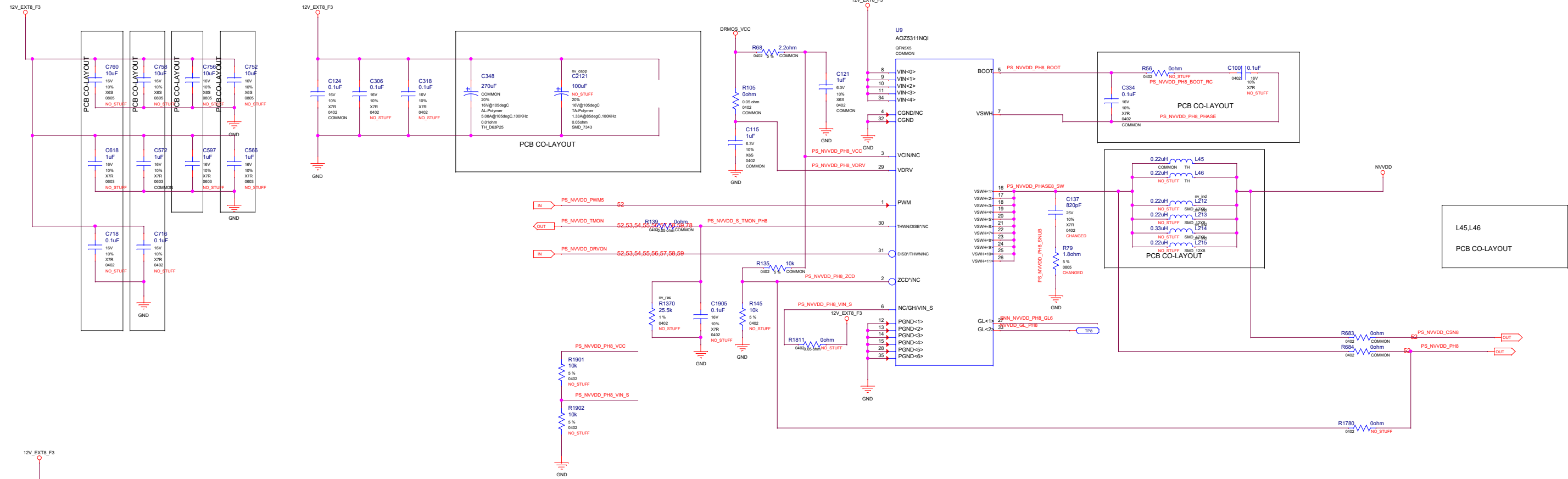
PS: NVVDD PH 5(PWM2), PH7(PWM3)



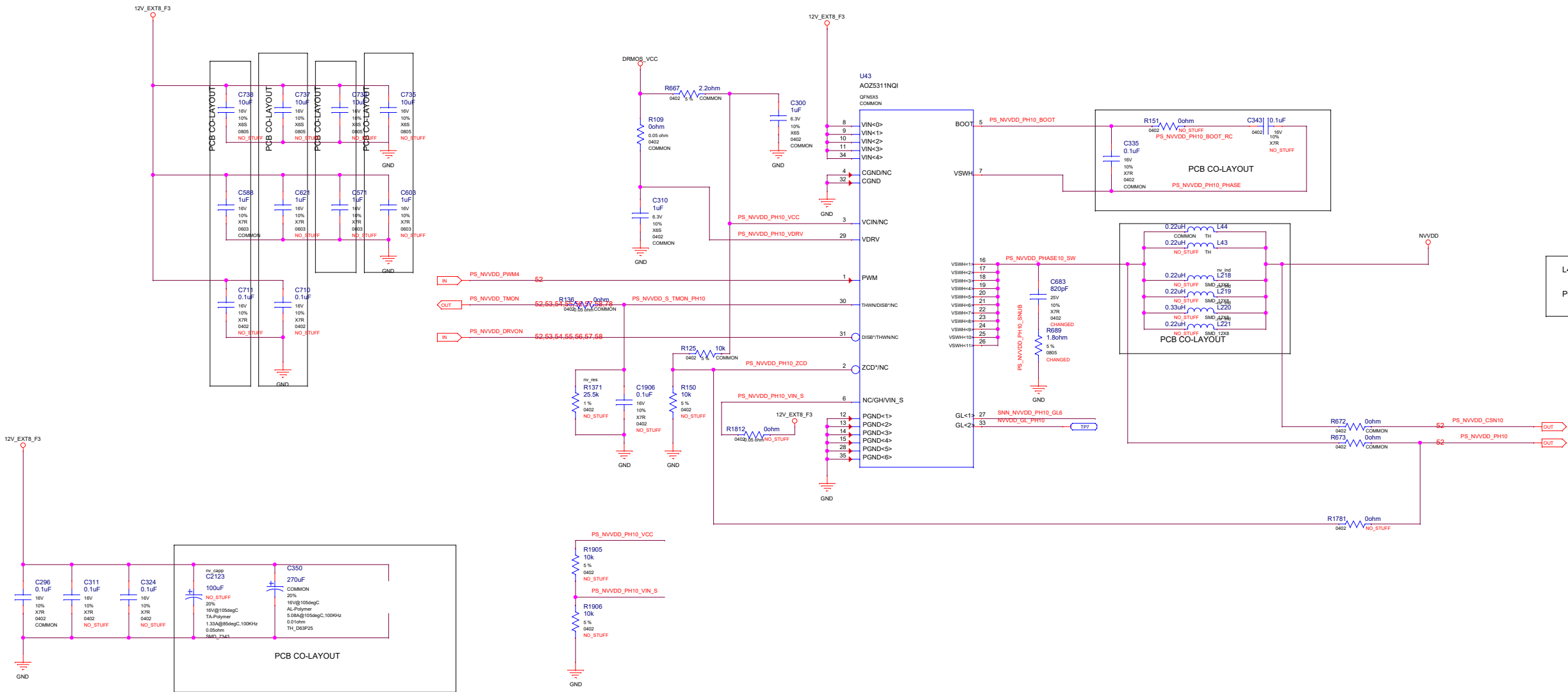
PS: NVVDD Phase 6(PWM7)



PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



PS: NVVDD Phase 10 (PWM8)



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PCB CO-LAYOUT

C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT


C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C256, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005


C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

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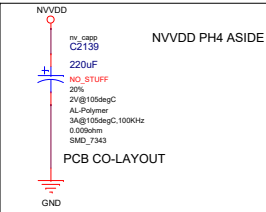
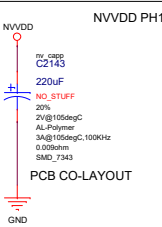
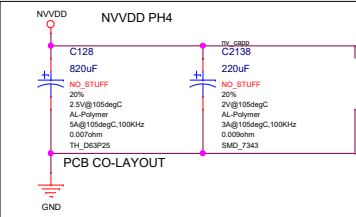
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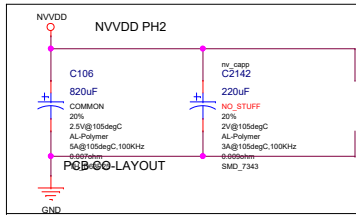
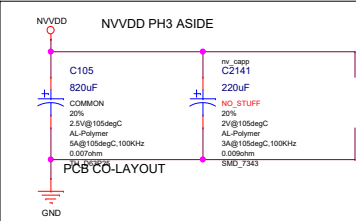
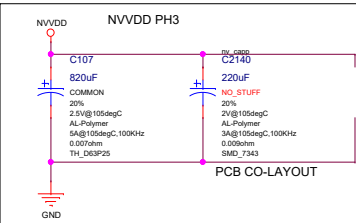
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Date: Tuesday, July 14, 2020		Sheet 61 of 79															
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PS: NVVDD OUTPUT CAP(TOP)

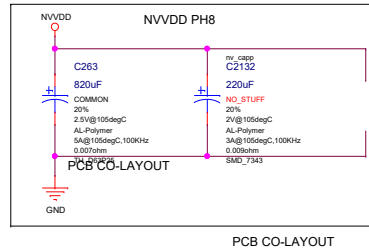
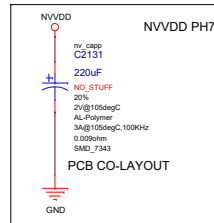
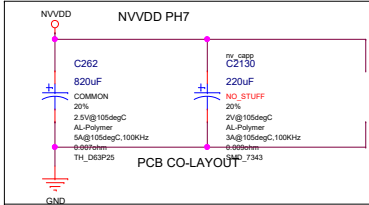
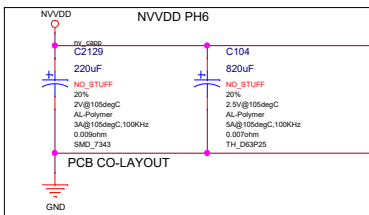
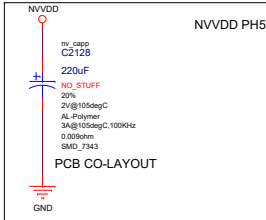


NV VDD PH1 ASIDE

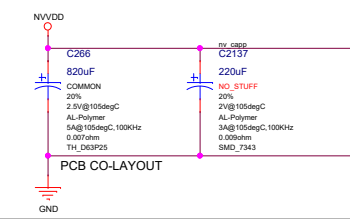
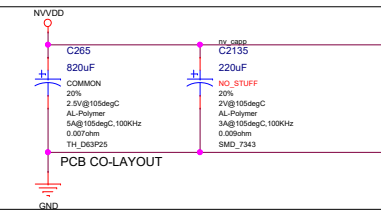
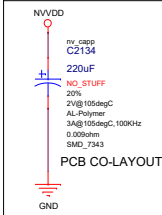
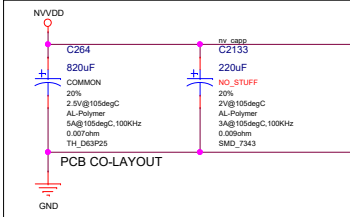
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PCB CO-LAYOUT



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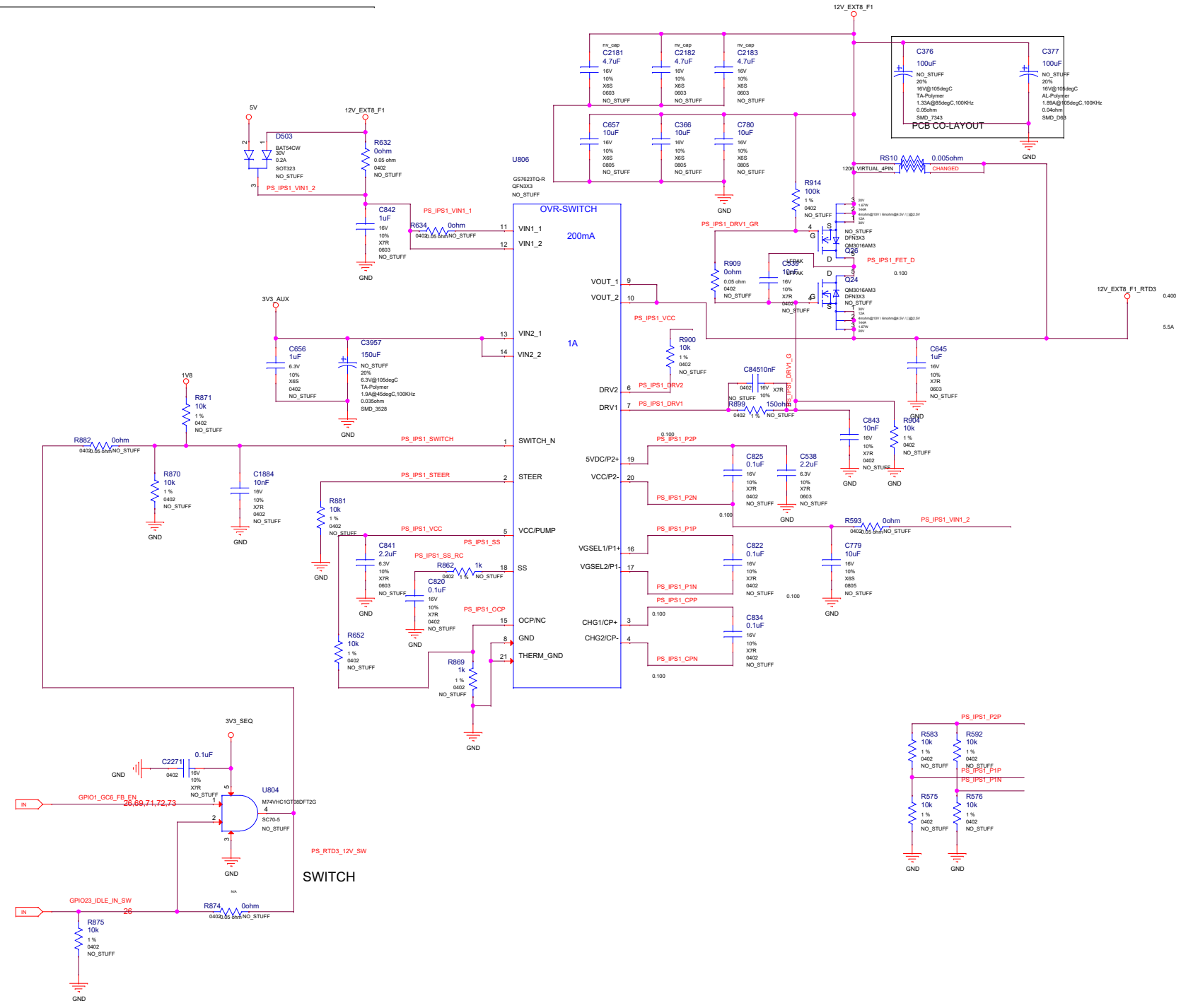
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PS: INPUT SWITCH RTD3


AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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PS: INPUT SWITCH
RTD3

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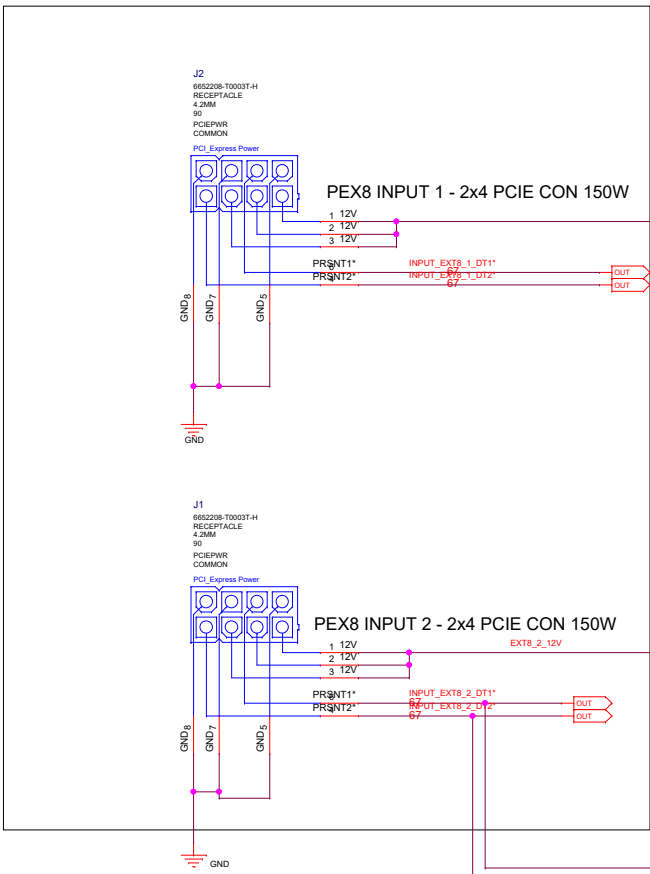
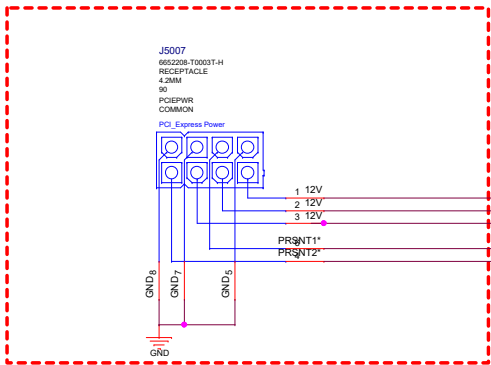
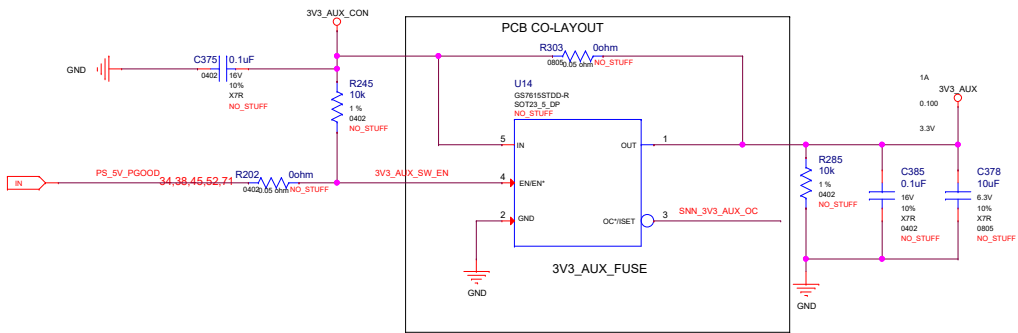
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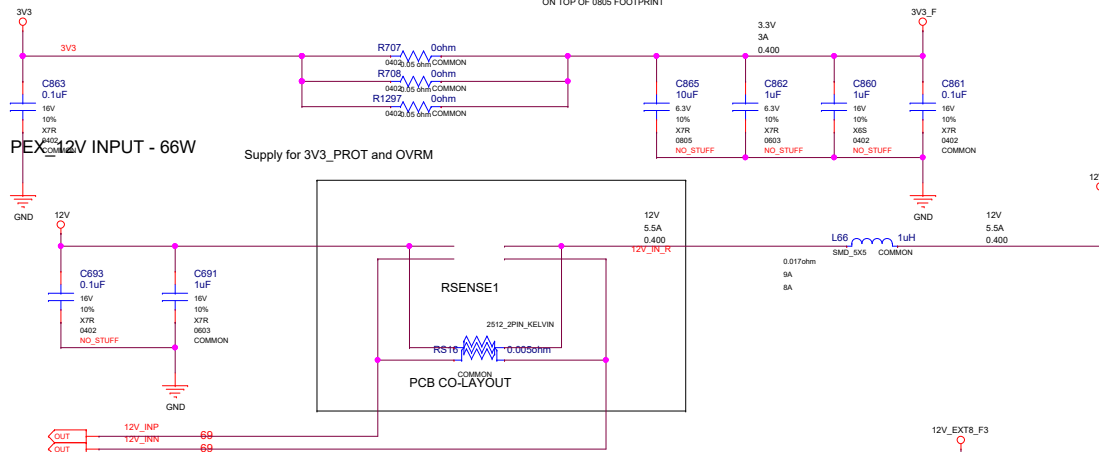
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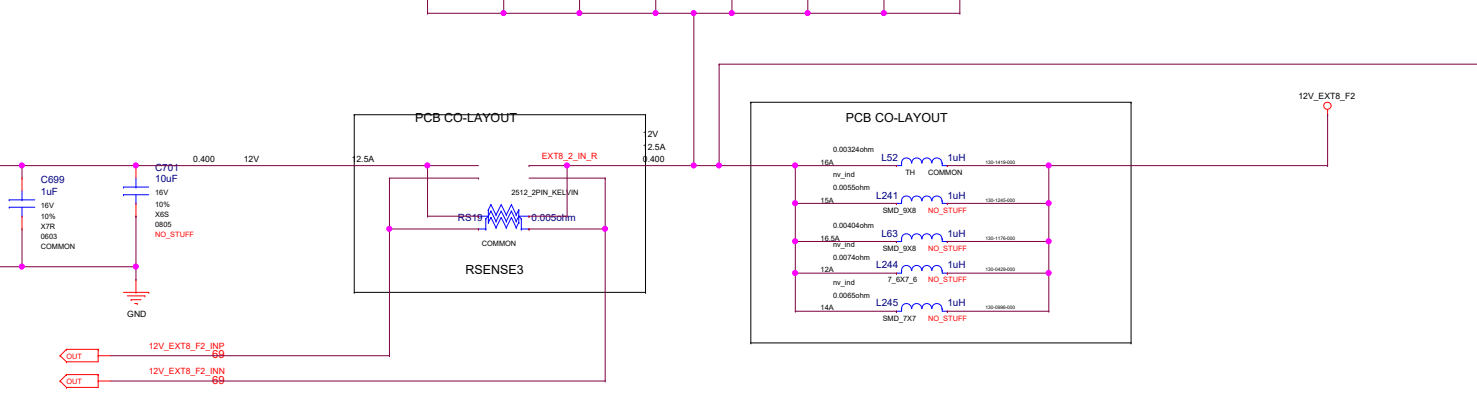
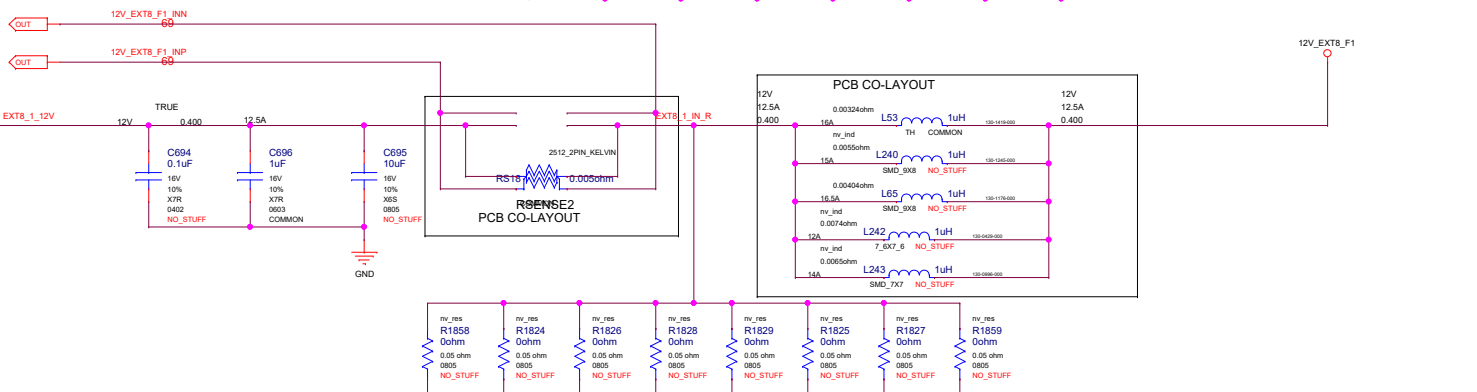
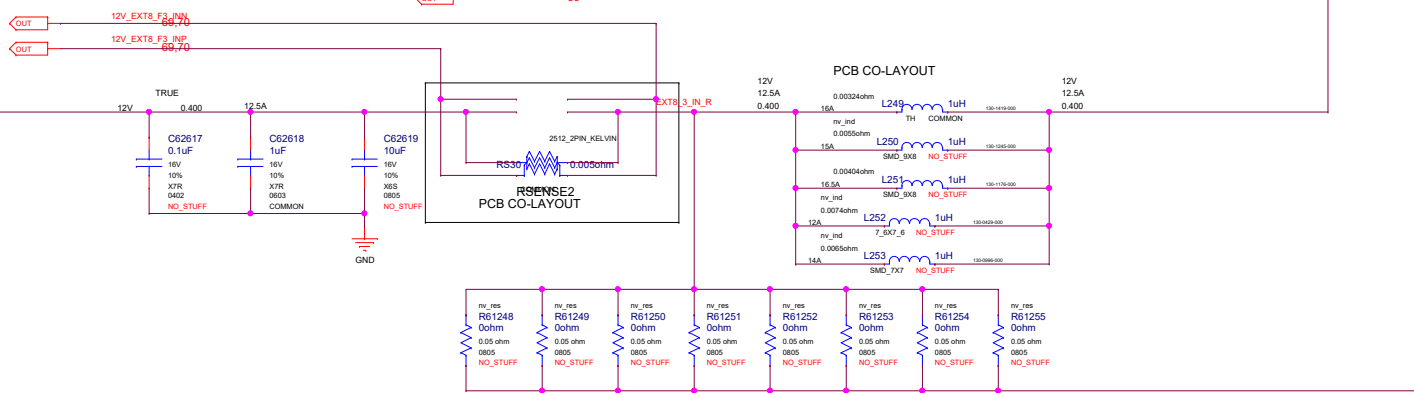
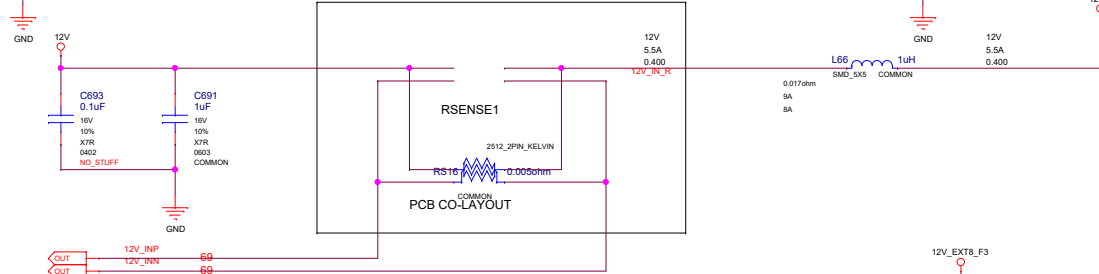
PS: Inputs, Filtering, and Monitoring



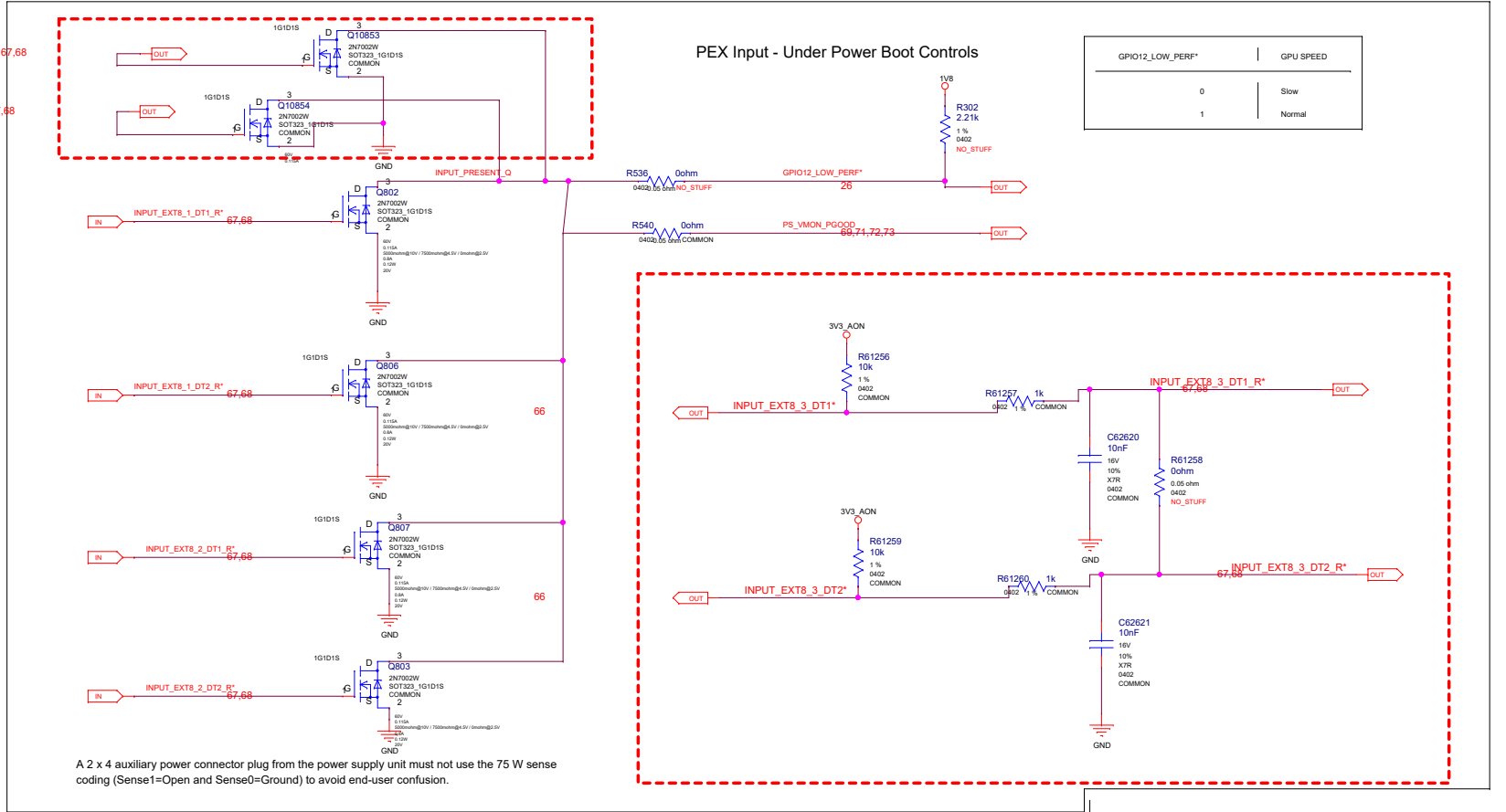
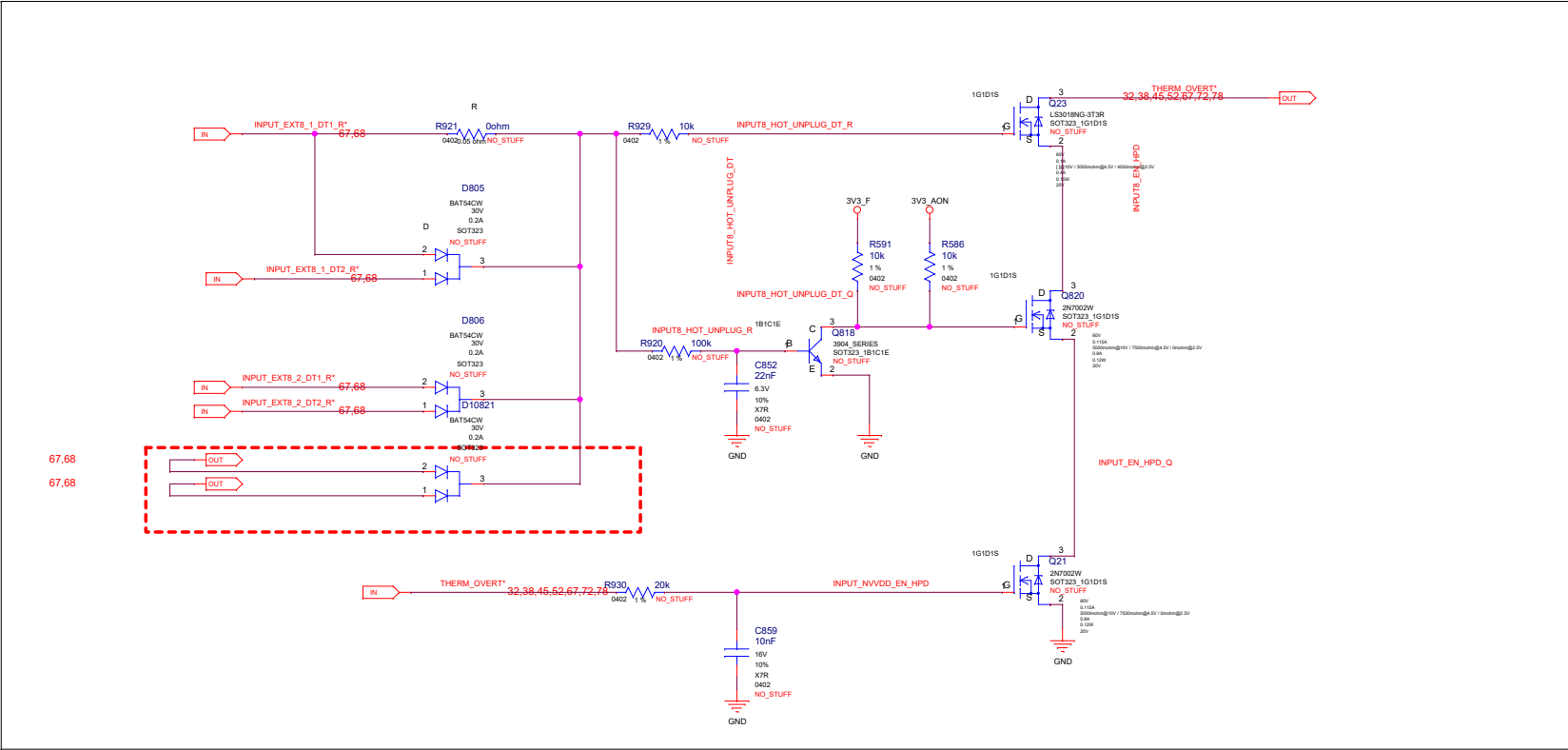
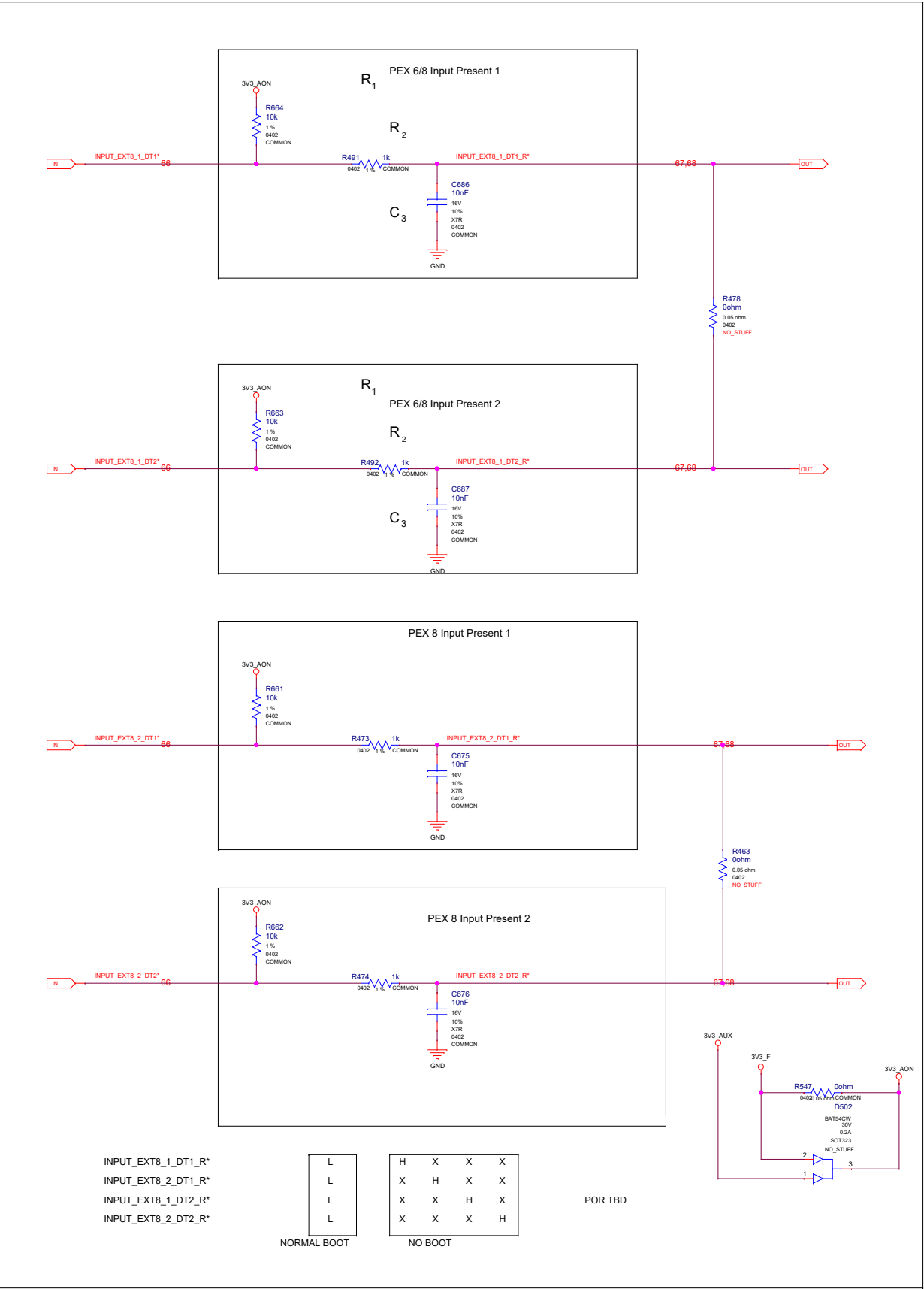
PEX 3V3 INPUT - 10W



PEX 12V INPUT - 66W



PS: 12V Current Steering & Hot Unplug Detect



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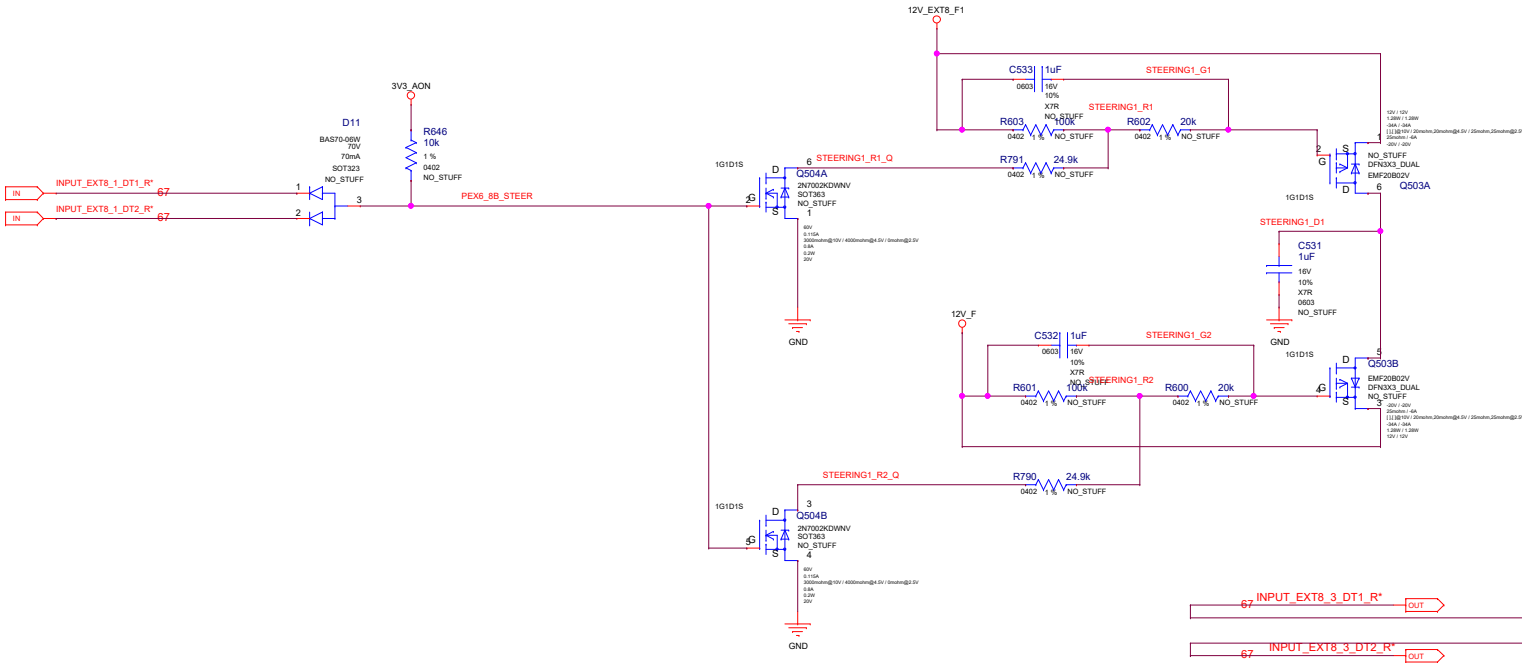
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PS: Discrete Steering

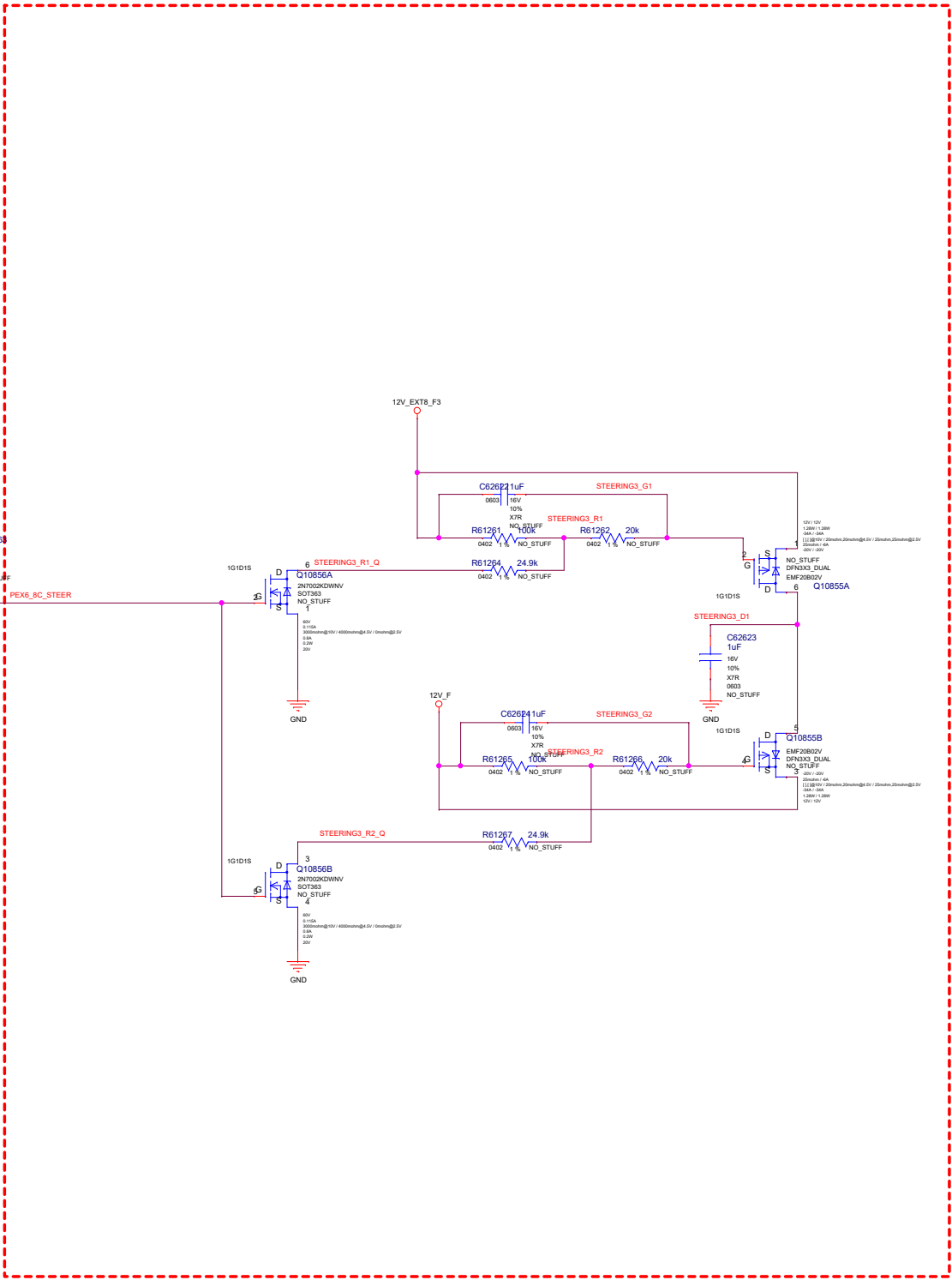
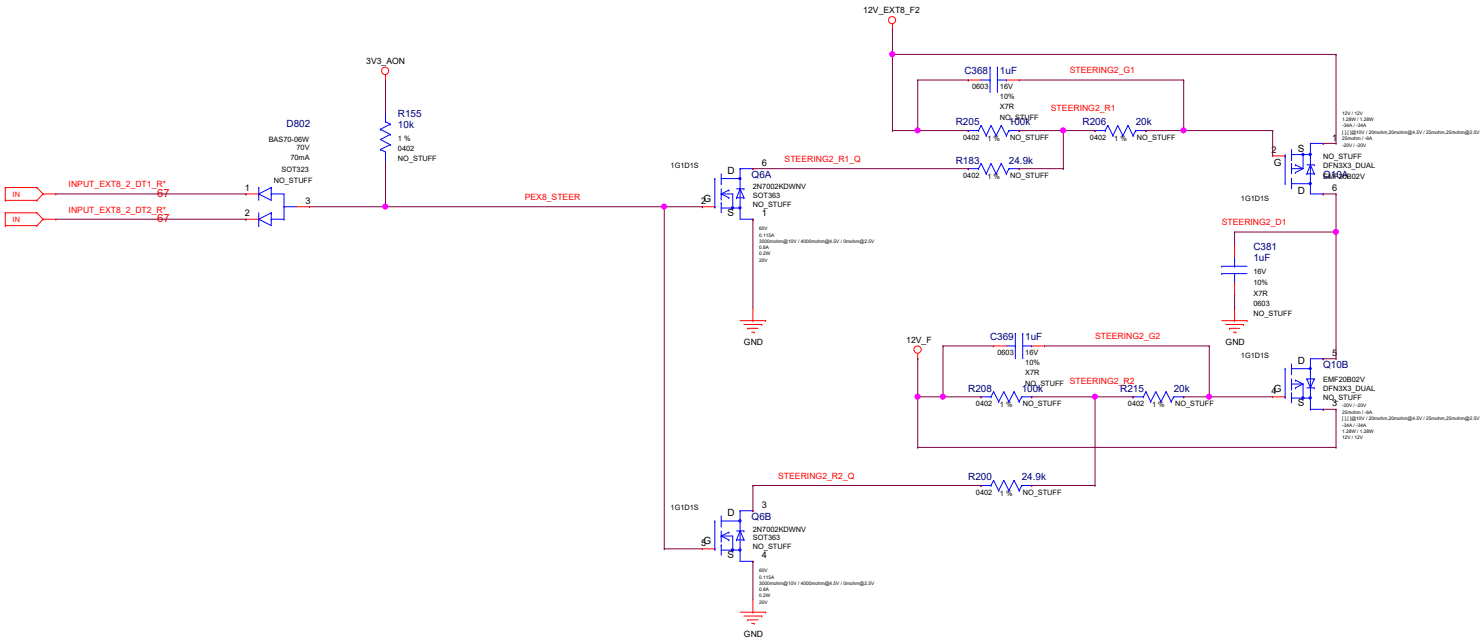
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1




NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



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PS: Pre-Filter

Route the trace to PEX Golden Finger



```
R841,R824,R816=modify 1K;
```

R444,R489,R498 modify

R452 add :19.6k

R818 add 1k

C814 ADD 1NF

R427 no_stuff

R368 ADD 1K

R334 DEL

R462 MODIFY TO 90.9K

R338 ADD 90.9K

Q265 3904 SOT323

R340 49.9k;

R369 ADD 10K

R360 MODIFY TO 10K

C382 ADD 1NF

Q255 ADD 2N7002 SOT363

R308 DEL



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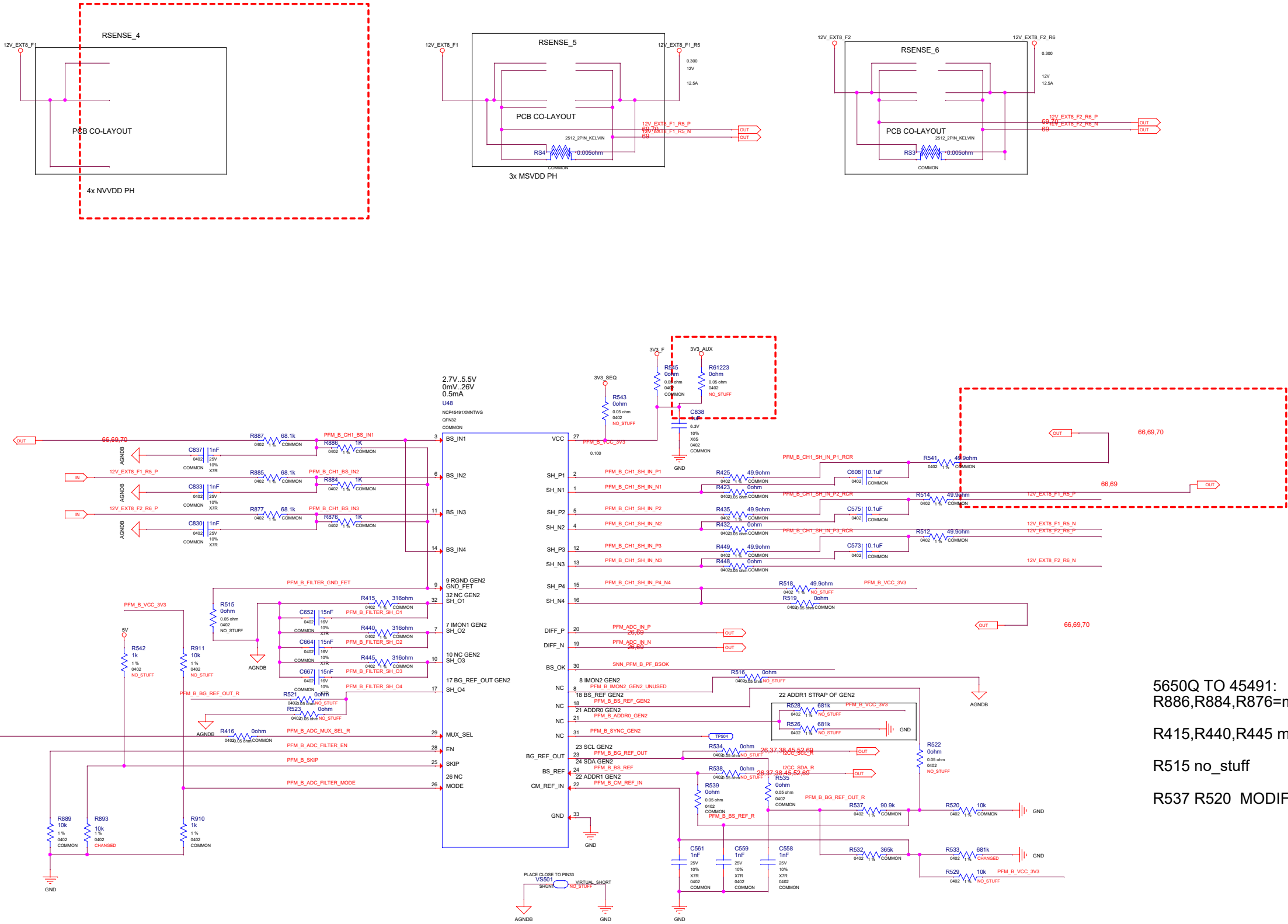
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PS: PREFILTER
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PS: Pre-Filter B



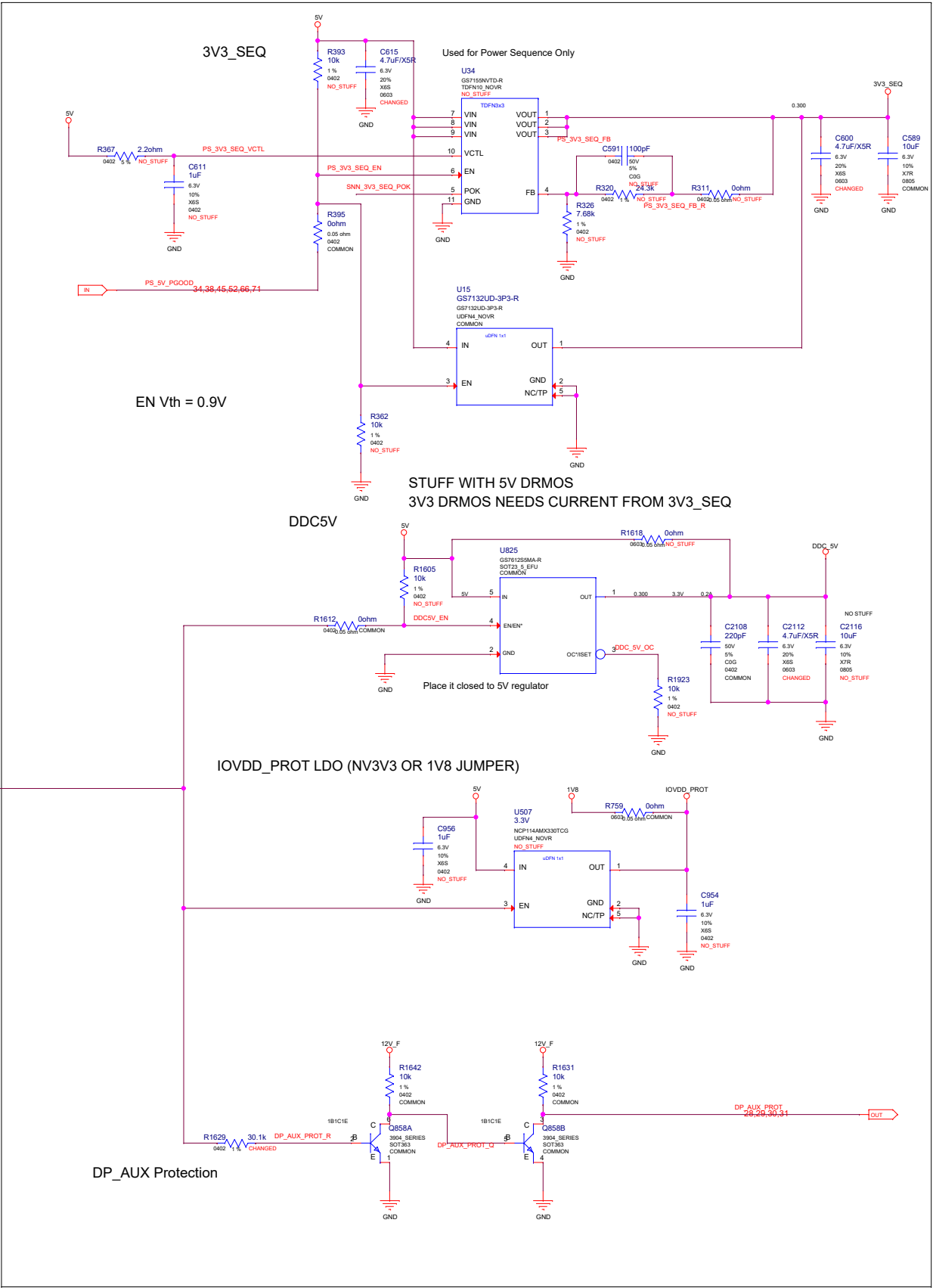
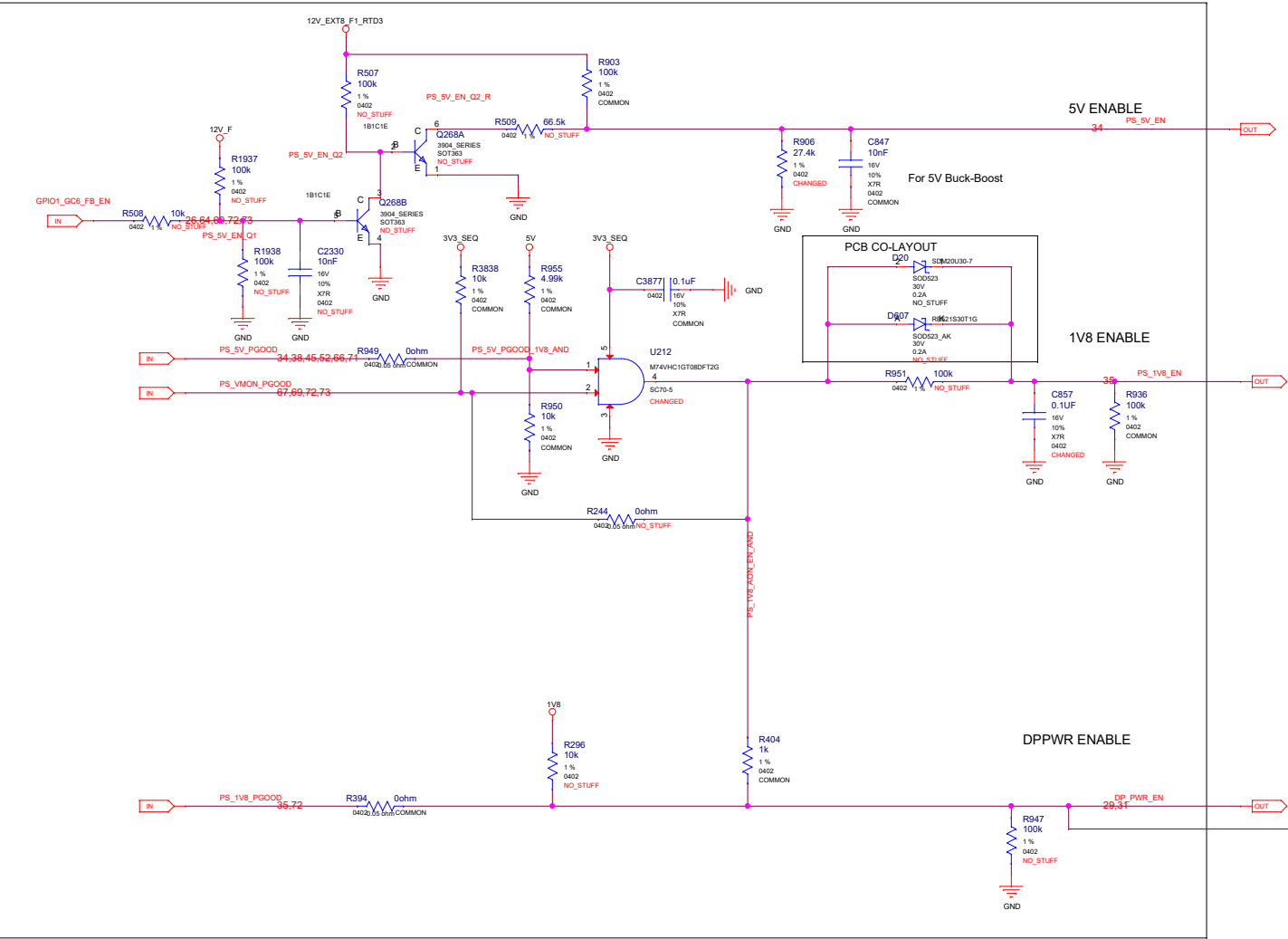
5650Q TO 45491:
R886,R884,R876=modify 1K;

R415,R440,R445 modify

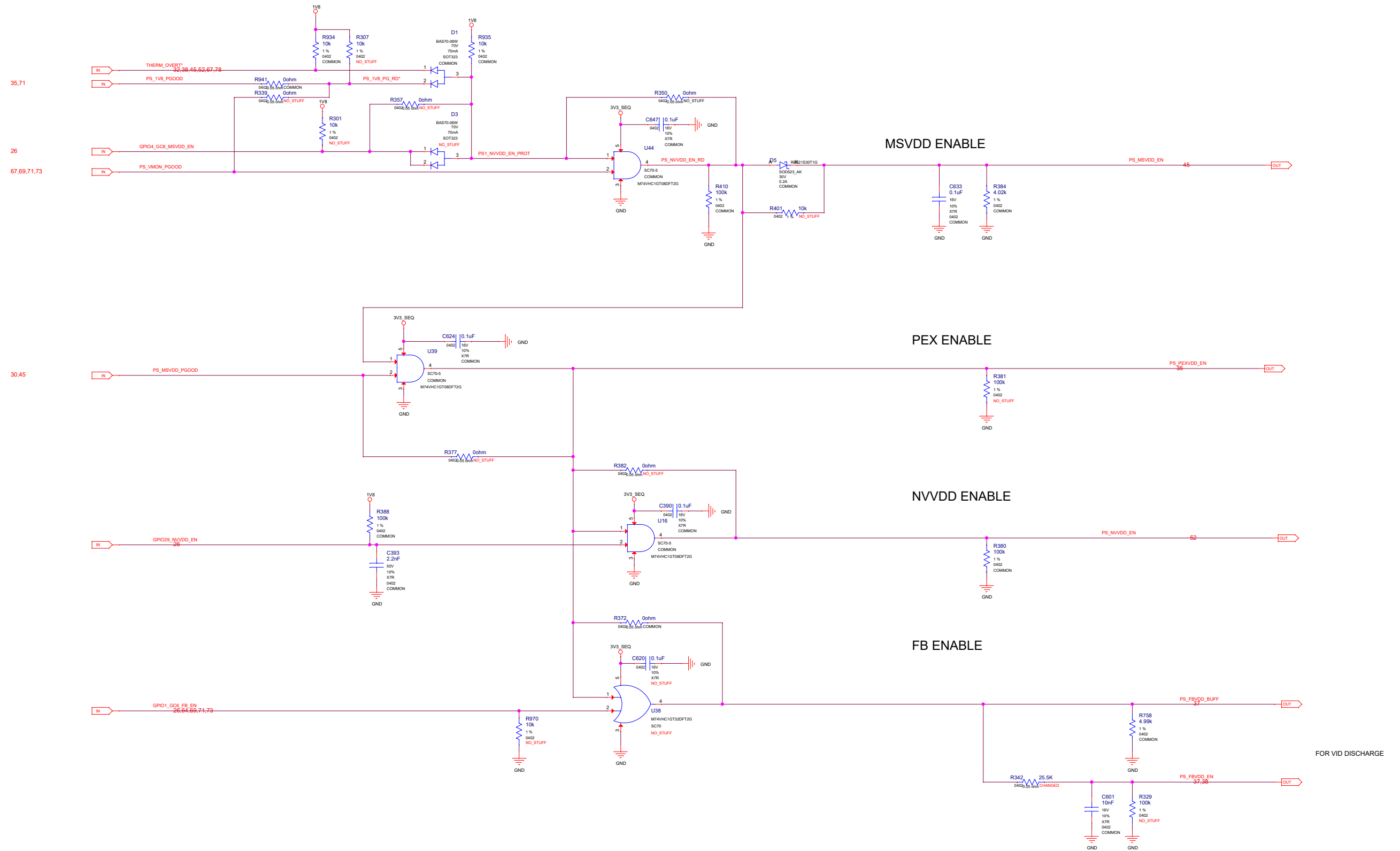
R515 no_stuff

R537 R520 MODIFY TO 90.9K

SEQUENCE:5V,1V8,3V3_SEQ ENABLE



SEQUENCE:NV,PEX,FB ENABLE



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PAGE DETAIL

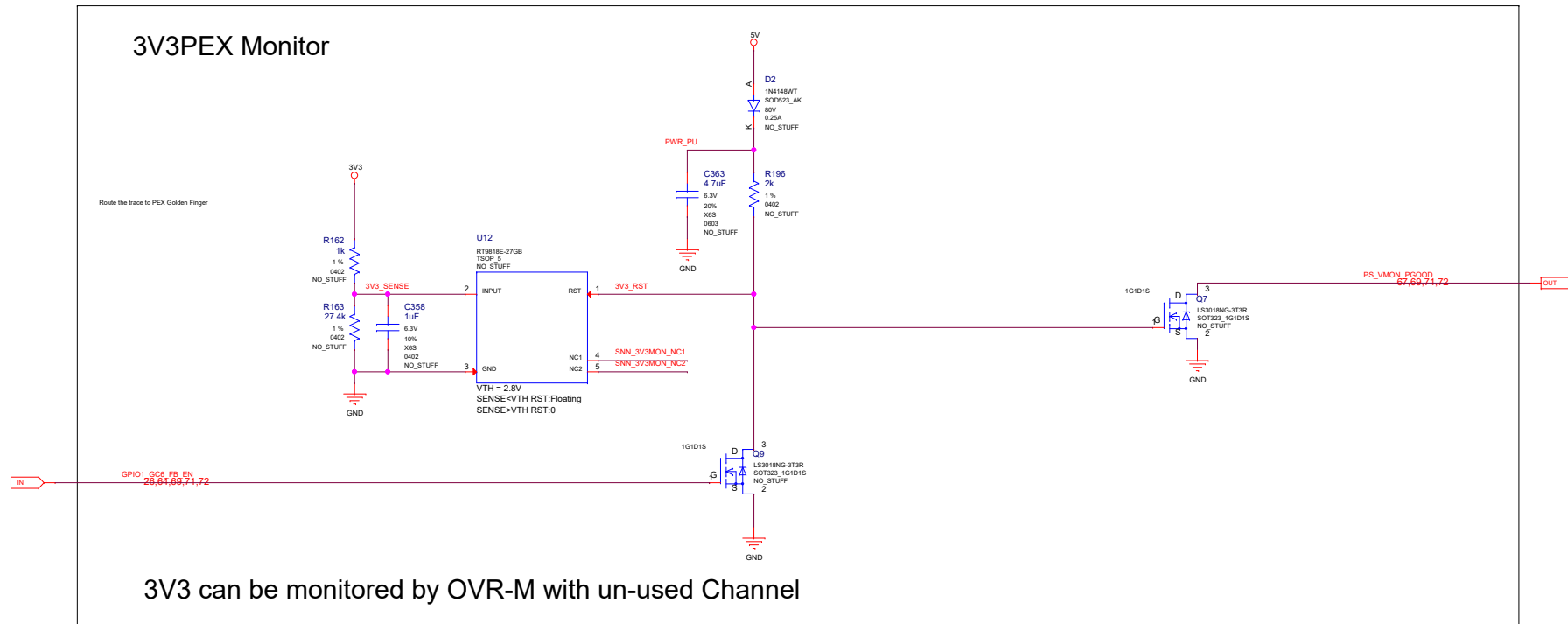
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Sequence: NV, PEX, FB EN



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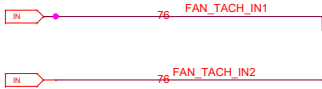
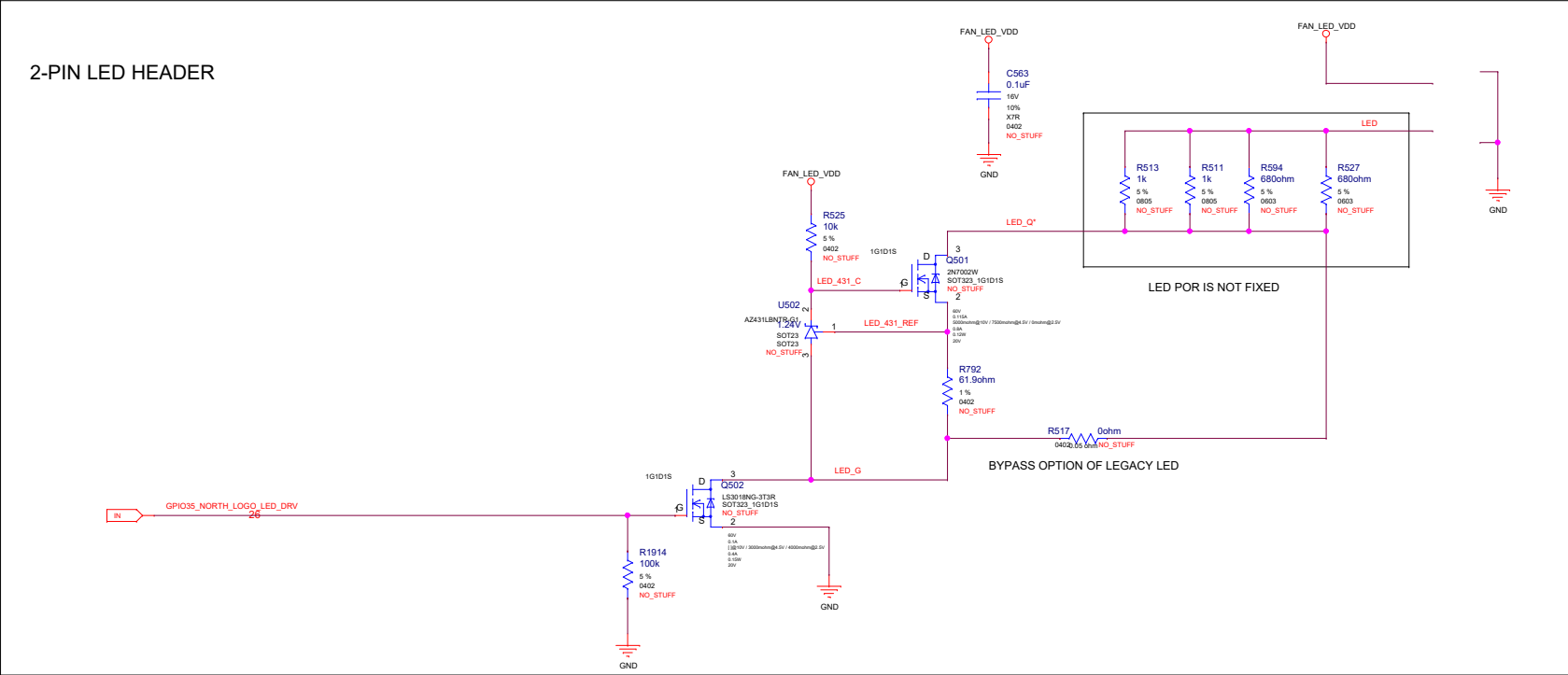
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Sequence: 3V3 MONITOR

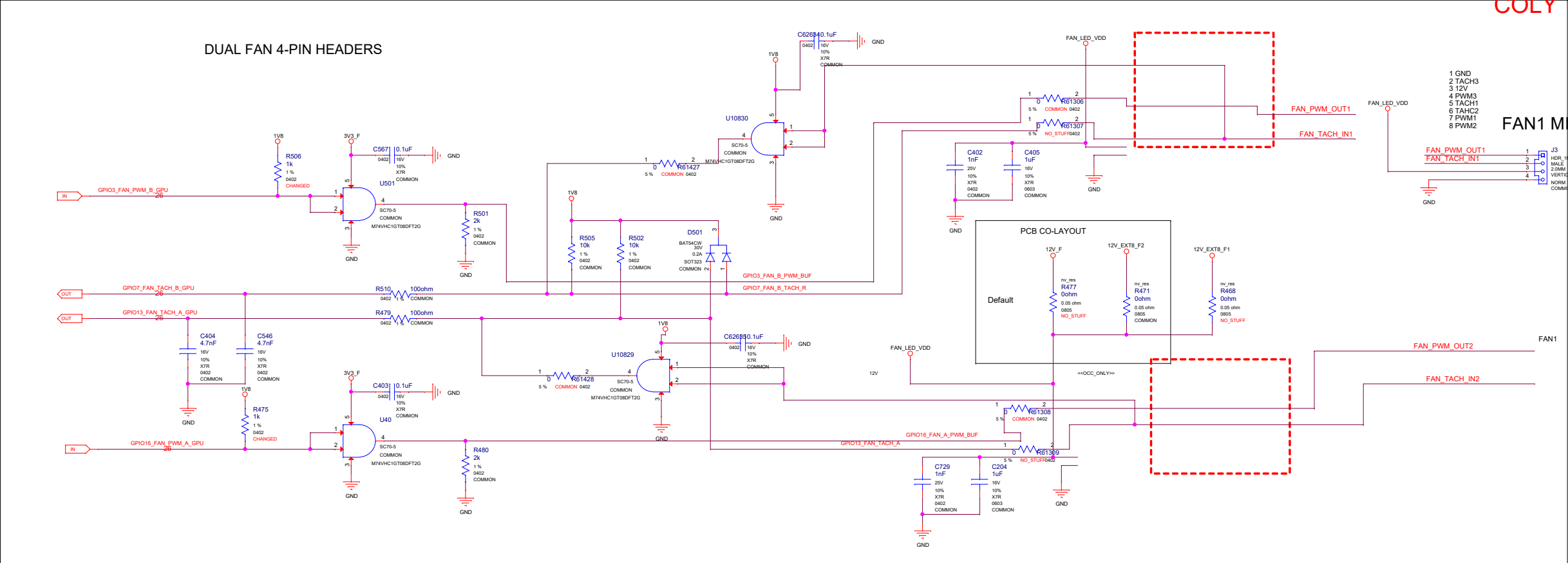


MISC: LED & FAN

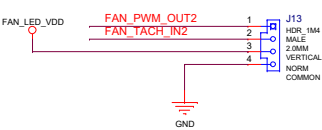
2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS

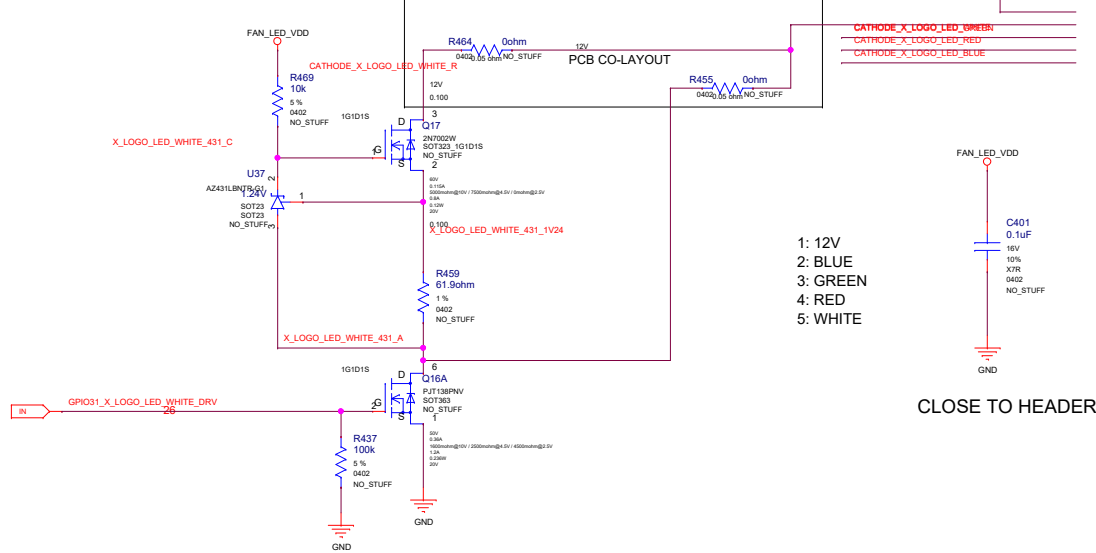


FAN0 FOR left&right middle fan



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MISC: RGBW LED REF

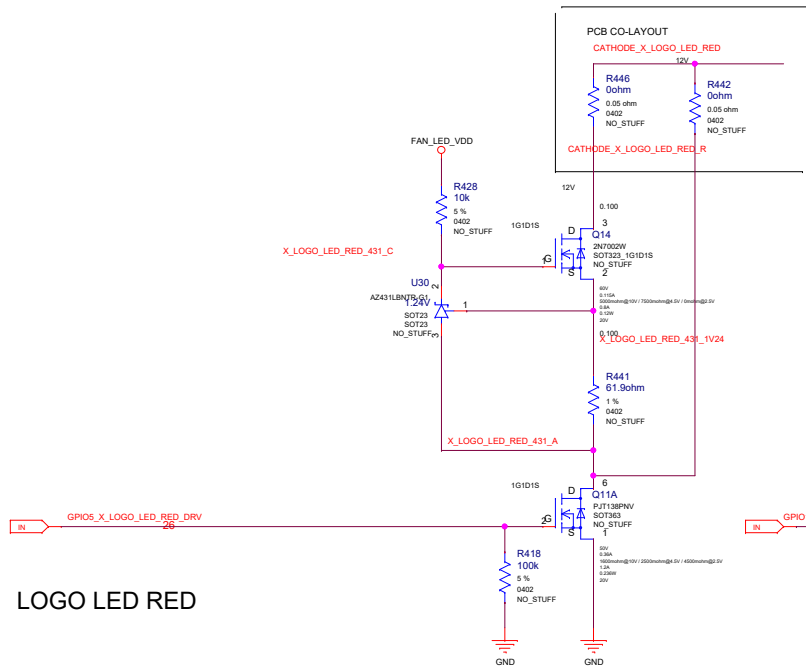


1: 12V
2: BLUE
3: GREEN
4: RED
5: WHITE

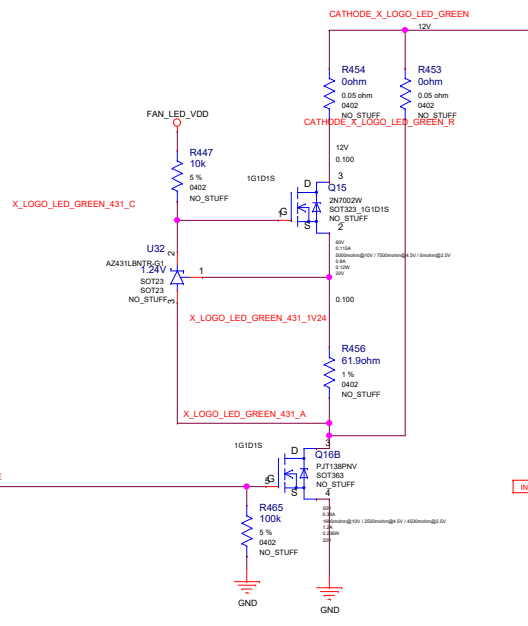
CLOSE TO HEADER

WHITE DRIVE

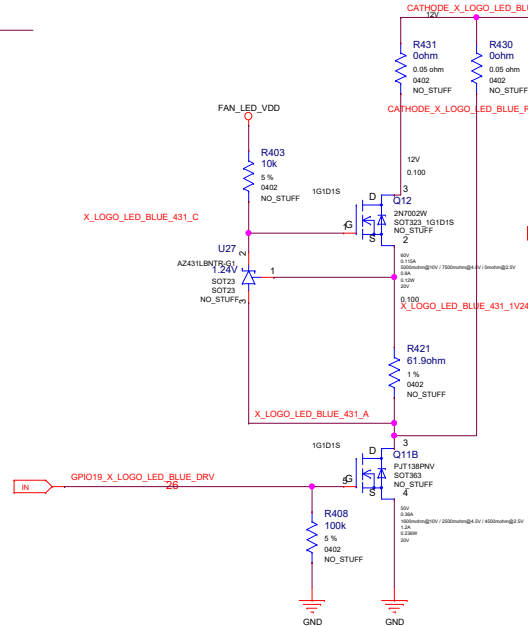
CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALIGN WITH PASH
IF ADDITIONAL POWER CONSUPTION R
NEEDED, IT SHOULD BE ON LED MOD.



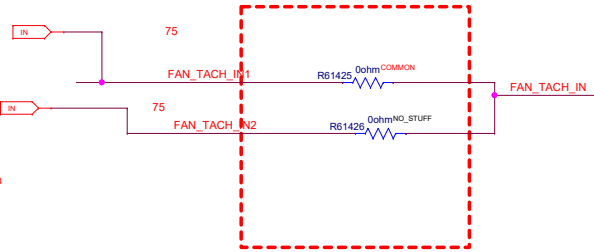
RED DRIVE



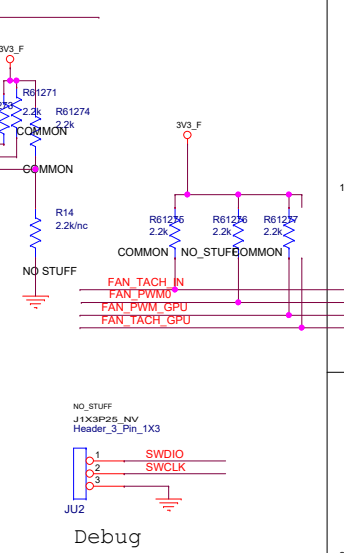
GREEN DRIVE



BLUE DRIVE

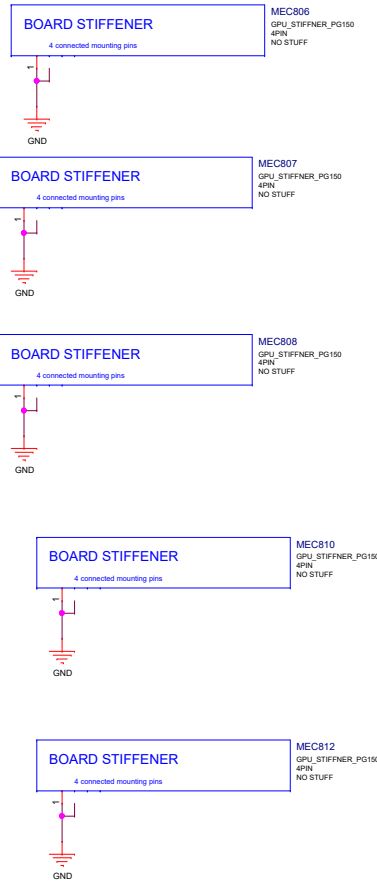
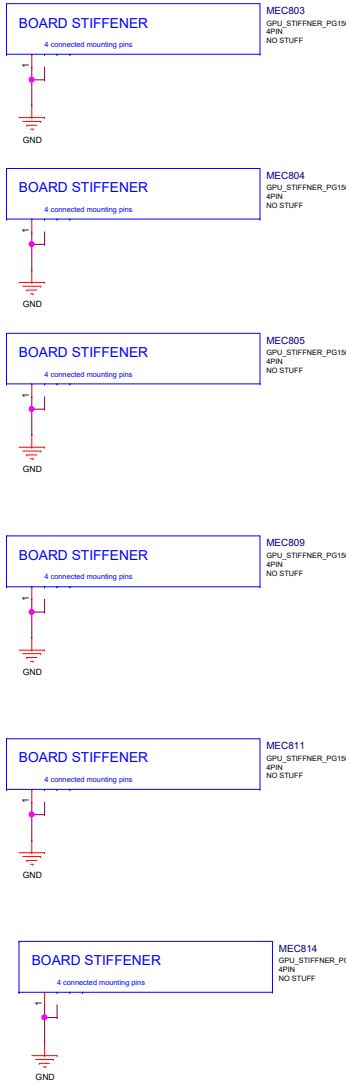
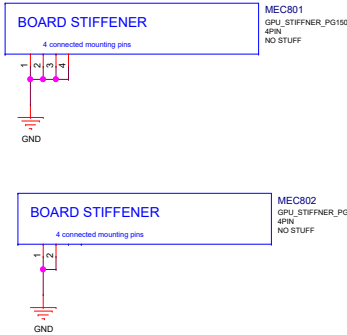
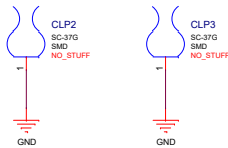


```
PA2  风扇转速侦测(有BUG, 需改成PA0或PA1)
PA3  MCU to GPU TACH
PA5  为LED电源控制口 高电压有效
PB0  风扇转速控制
PB2  MCU to GPU PWM
PB1  LED_RED
PB3  LED_GREEN
PB4  LED_BLUE
```



Debug

Mechanical: Mounting holes

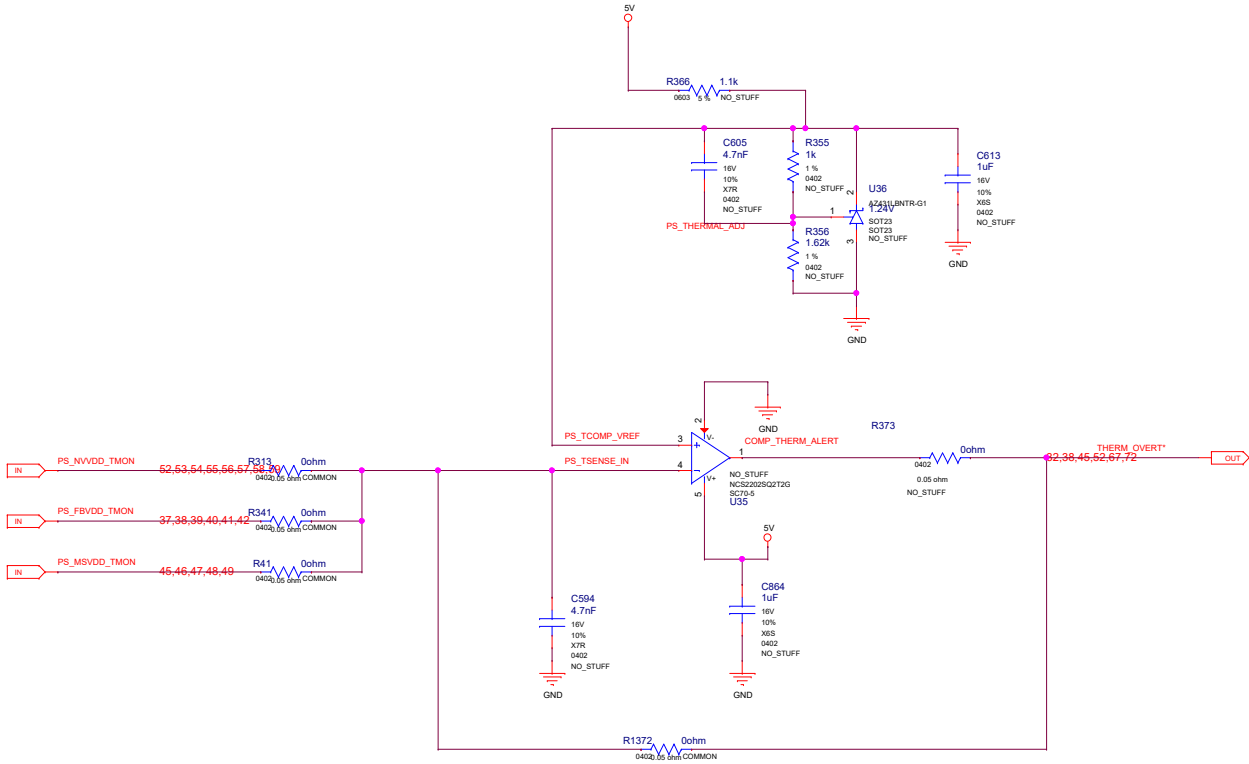


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VR THERMAL PROTECTION



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VR Thermal
Protection

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PCI TERM



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